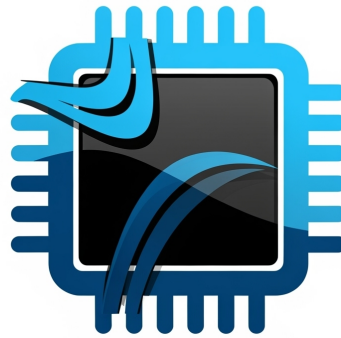




Integrated development environment for teaching and research on RISC-V processors
(PDC2023-145832-I00)

Integrated development environment for teaching and research on RISC-V processors



CREATOR

D 2.1

User manual, use cases, and materials for
CREATOR and Sail specification

Universidad Carlos III de Madrid

January, 2026

CONTENTS

USER MANUAL AND USE CASES	1
Architecture guides	1
RISC-V architecture	1
System calls.	2
Interrupts	2
MIPS architecture	3
Overview	3
System calls.	5
CLI User Guide	6
Installation.	6
Installing CREATOR CLI	6
Getting Architecture Files	8
Configuration	8
Updating	8
Command-Line Options	9
Basic Usage.	9
Required Options.	9
Input Options.	9
Assembler Options	10
Other Options	11
Getting Help	12
Commands Reference	12
Execution Control	13
Breakpoint Management	18
Inspection Commands	19
State Management	24
Utility Commands	25
Command Aliases.	27
Keyboard Shortcuts.	28

Configuration	28
Configuration File Location.	28
Configuration Structure.	28
Settings Section.	29
Aliases Section	30
Shortcuts Section	31
Complete Example Configuration.	32
Configuration Loading	34
Teaching Resources	35
Setting up the Remote Laboratory	35
Setup and configuration	35
CREATOR API (CAPI).	37
Memory.	37
System calls.	38
Validation.	40
Stack	41
Floating point.	41
Registers	44
Architecture	44
Interrupts	54
Creating Custom Architectures	57
Creating an Architecture File.	57
Plugins	63
Interrupt Support.	63
Privileged instructions	70
Validating program execution	71
Validator File	72
Web Version Overview	74
Access.	74
Features.	74
User Interface	75
Architecture Select View	75
Editor View.	75

Simulator View	76
Architecture View	80
Settings Menu	83
CREATOR Remote Laboratory	84
User Interface	85
Editor Features	86
Syntax Highlighting	87
Auto-Completion (IntelliSense)	87
Help Tooltips	87
Go to Definition/References	87
Code Comments	87
Minimap	88
Error and Warning Indicators	89
Vim Mode	89
CREATOR Gateway	89
Supported devices	89
Executing the ESP32 gateway	91
Executing the SBC gateway	98
User Interface	99
Execution Control	100
Execution Controls	100
Breakpoints	101
Execution Modes	101
Interrupt Handling	101
Assemblers	102
CREATOR Assembler	102
RASM	103
Choosing an Assembler	103
CREATOR Arduino module (CREATino)	103
Using CREATino library functions	103
Examples	104
Example 2: Button + LED	106
Example 3: Text input/output using serial output	113

Example 4: Daytime running lights with <code>analogRead</code>	116
Example 5: [Advanced] Piano	119
USER MANUAL AND USE CASES FOR THE SAIL-BASED MODEL.	126
User manual	126
Init page	126
Simulation module	128
Code editor module.	131
Program execution in the web simulator	132
Use cases with the new functionalities of the simulation tool.	134
Execution of a program with a custom kernel coded in assembly language.	134
Execution of a program with vector instructions..	135
Execution of a program compiled with a library which was previously generated.	136

USER MANUAL AND USE CASES

Architecture guides

RISC-V architecture

CREATOR supports RISC-V 32-bits and 64-bits full specification through Sail, but also has a 32/64-bits standalone build-in partial specification with the I, M, F, and D extensions. A quick reference guide of this partial specification is available at: <https://creatorsim.github.io/creator/guides/riscv.pdf>.

RISC-V Reference Guide (CREATOR Simulator)

System Calls (ecall)				Integer Registers	
Service	Call Code (e7)	Arguments	Result	Register Name	Usage
Print_int	1	a0 = integer		zero	Constant 0
Print_float	2	fa0 = float		ra	Return address (routines/functions)
Print_double	3	fa0 = double		sp	Stack pointer
Print_string	4	a0 = string addr		gp	Global pointer
Read_int	5		Integer in a0	tp	Thread pointer
Read_float	6		Float in fa0	t0..t6	Temporary (NOT preserved across calls)
Read_double	7		Double in fa0	s0..s11	Saved temporary (preserved across calls)
Read_string	8	a0 = string addr a1 = length		a0, a1	Arguments for functions / return value
Sbrk	9	a0 = length	Address in a0	a2..a7	Arguments for functions
Exit	10			Floating-point registers	
Print_char	11	a0 = ASCII code		ft0..ft11	Temporary (NOT preserved across calls)
Read_char	12		Char in a0	fs0..fs11	Saved temporary (preserved across calls)
				fa0, fa1	Arguments for functions / return value
				fa2..fa7	Arguments for functions

Data transfer		Arithmetic (floating point, s/d)	
li rd, n	rd = n (PseudoInst, n-> 32 bits)	fmv.s fd, fs1	fd = fs1
mv rd, rs	rd = rs	fadd.s fd, fs1, fs2	fd = fs1+fs2
lui rd, imm	rd = imm[31:12] <<12 (extend the sign)	fsub.s fd, fs1, fs2	fd = fs1-fs2
Arithmetic (Integer)		fmul.s fd, fs1, fs2	fd = fs1*fs2
add rd, rs1, rs2	rd = rs1+rs2	fdiv.s fd, fs1, fs2	fd = fs1/fs2
addi rd, rs1, n	rd = rs1 + n (n-> 12 bits)	fmin.s fd, fs1, fs2	fd = min(fs1, fs2)
sub rd, rs1, rs2	rd = rs1 - rs2	fmax.s fd, fs1, fs2	fd = max(fs1, fs2)
mul rd, rs1, rs2	rd = rs1*rs2	fsqrt.s fd, fs1	fd = sqrt(fs1)
div rd, rs1, rs2	rd = rs1/rs2	fnadd.s fd, fs1, fs2, fs3	fd = fs1*fs2+fs3
rem rd, rs1, rs2	rd = rs1%rs2	fmsub.s fd, fs1, fs2, fs3	fd = fs1*fs2-fs3
Logical (Integer)		fabs.s fd, fs1	fd = fs1
and rd, rs1, rs2	rd = rs1 AND rs2	fneg.s fd, fs1	fd = -fs1
andi rd, rs1, n	rd = rs1 AND n (n-> 12 bits)	Integer <-> Floating point	
or rd, rs1, rs2	rd = rs1 OR rs2	fmv.w.x fd, rs	fd = rs single = integer
ori rd, rs1, n	rd = rs1 OR n (n-> 12 bits)	fmv.w rd, fs	rd = fs integer = single
not rd, rs1	rd = !rs1 (one's complement)	Comparison (Integer, n-> 12 bits)	
neg rd, rs1	rd = rs1 + 1 (two's complement)	slt rd, rs1, rs2	if (rs1 < rs2) rd = 1; else rd = 0
xor rd, rs1, rs2	rd = rs1 XOR rs2	sltu rd, rs1, rs2	if (u(rs1) < u(rs2)) rd = 1; else rd = 0
srl rd, rs1, n	rd = rs1 >> n logical, n-> 5 bits	slti rd, rs1, n	if (s(rs1) < s(n)) rd = 1; else rd = 0
sll rd, rs1, n	rd = rs1 << n n-> 5 bits	sltiu rd, rs1, n	if (u(rs1) < u(n)) rd = 1; else rd = 0
srai rd, rs1, n	rd = rs1 >> n arithmetic, n-> 5 bits	sgeq rd, rs1	if (rs1 >= 0) rd = 1; else rd = 0
sra rd, rs1, rs2	rd = rs1 >> rs2 arithmetic	snez rd, rs1	if (rs1 != 0) rd = 1; else rd = 0
sll rd, rs1, rs2	rd = rs1 << rs2	sgtz rd, rs1	if (rs1 > 0) rd = 1; else rd = 0
srl rd, rs1, rs2	rd = rs1 >> rs2 logical	sltz rd, rs1	if (rs1 < 0) rd = 1; else rd = 0
Branch Instructions (Integer registers)		Comparison (Floating point)	
beq t0, t1, etiq	Jump to etiq if t0==t1	(rd=Int register, fs1 and fs2 floating point register)	
bne t0, t1, etiq	Jump to etiq if t0!=t1	feq.s rd, fs1, fs2	if (fs1==fs2) rd=1;else rd=0 (float)
bit t0, t1, etiq	Jump to etiq if t0<t1	fle.s rd, fs1, fs2	if (fs1<=fs2) rd=1;else rd=0 (float)
bltu t0, t1, etiq	Jump to etiq if t0<t1 (unsigned)	flt.s rd, fs1, fs2	if (fs1<fs2) rd=1;else rd=0 (float)
bge t0, t1, etiq	Jump to etiq if t0>=t1 (unsigned)	feq.d rd, fs1, fs2	if (fs1==fs2) rd=1;else rd=0 (double)
bgtu t0, t1, etiq	Jump to etiq if t0>t1 (unsigned)	fle.d rd, fs1, fs2	if (fs1<=fs2) rd=1;else rd=0 (double)
bgt t0, t1, etiq	Jump to etiq if t0>t1	flt.d rd, fs1, fs2	if (fs1<fs2) rd=1;else rd=0 (double)
bgtu t0, t1, etiq	Jump to etiq if t0>t1 (unsigned)	Function Calls	
ble t0, t1, etiq	Jump to etiq if t0<=t1	jal ra, address	ra = PC; PC = address
bleu t0, t1, etiq	Jump to etiq if t0<=t1 (unsigned)	jr ra	PC = ra
j etiq	PC = PC + etiq	Hardware Counter	
Memory Access (Integer registers), n->12 bits		rdcycle rd	rd = number of elapsed cycles
la rd, address	rd = Memory[address] load 32 bits	Memory access (floating point), n->12bits	
lb rd, n(rs1)	rd = Memory[n+rs1] load byte	flw fd, n(rs1)	fd = Memory[n+rs1] load float
lbu rd, n(rs1)	rd = Memory[n+rs1] load byte unsigned	fsw fd, n(rs1)	Memory[n+rs1] = fd store float
lw rd, n(rs1)	rd = Memory[n+rs1] load word	fld fd, n(rs1)	fd = Memory[n+rs1] load double
sb rd, n(rs1)	Memory[n+rs1] = rd store byte	fsd fd, n(rs1)	Memory[n+rs1] = fd store double
sw rd, n(rs1)	Memory[n+rs1] = rd store word		

Conversion Operations		Floating-point Classification	
fcvt.w.s rd, fs1	From single precision (fs1) to integer (rd) with sign	fclass.s rd, fs1	Classify single precision
fcvt.wu.s rd, fs1	From single precision (fs1) to integer (rd) without sign	fclass.d rd, fs1	Classify double precision
fcvt.s.w fd, rs1	From integer with sign (rs1) to single precision (fd)	BIT position in rd	
fcvt.s.wu fd, rs1	From integer without sign (rs1) to single precision (fd)	0, 7	-Inf, +Inf
fcvt.w.d rd, fs1	From rom double precision (fs1) to integer (rd) with sign	1	Normalized negative
fcvt.wu.d rd, fs1	From double precision (fs1) to integer (rd) without sign	2	Not normalized negative
fcvt.d.w fd, rs1	From integer with sign (rs1) to double precision (fd)	3, 4	-0, +0
fcvt.d.wu fd, rs1	From integer without sign (rs1) to double precision (fd)	5	Non normalized positive
fcvt.s.d fd, fs1	From double (fs1) to single precision (fd)	6	Normalized positive
fcvt.d.s fd, fs1	From single (fs1) to double precision (fd)	8, 9	Signaling NaN, Quiet NaN



System calls

The supported system calls are the following:

Service	Trap Code	Input	Output	Notes
print_int	a7 = 1	a0 = int to be printed	Print a0 to display	
print_float	a7 = 2	fa0 = float to be printed	Print fa0 to display	
print_double	a7 = 3	fa0 = double to be printed	Print fa0 to display	
print_string	a7 = 4	a0 = 1st char's address	Print string in the display	
read_int	a7 = 5		Read integer in a0	
read_float	a7 = 6		Read float to fa0	
read_double	a7 = 7		Read double to fa0	
read_string	a7 = 8	a0 = buffer address, a1= buffer length	Read string	
sbrk	a7 = 9	a0 = number of bytes	a0 points to the allocated memory	Allocation from heap
exit	a7 = 10			End of execution
print_char	a7 = 11	a0 = ASCII code	Print a0 to display	
read_char	a7 = 12		Read char to a0	

Interrupts

The RISC-V-32 ISA defines different privilege modes that determine the level of access and control a process has over the system's resources levels, in particular, access to *Control Status Registers* (CSRs), the privileged instruction set, and privileged ISA extensions. The instruction subset to control CSRs is provided in the *Zicsr* extension.

The ISA defines three levels: User/Application (U), Supervisor (S), and Machine (M), allowing implementations to provide one, two, or three of them (There are only three supported combinations: M-level, M-level and U-level, or all three). M-level is the highest privilege level, while U-level is intended for conventional applications and S-level for operating systems.

RISC-V handles exceptions and interrupts by generating traps. As a trap involves elevating the privilege level, e.g. requesting an OS system call from a user program, both M and S privilege levels include a set of CSRs for handling them ¹. The `mstatus` (*Machine Status*) register keeps track of and controls the CPU's current operating state. In this register, there are several interrupt-related fields: field `MIE` (*Machine Interrupt Enable*) controls whether interrupts are globally enabled or disabled for that privilege mode, field `MPP` (*Machine Previous Privilege Mode*) holds the previous privilege mode, and, to allow nesting of interrupts, field `MPPIE` stores the previous value of `MIE` when an interrupt occurs.

¹As they are virtually the same, only the M-level set will be described.

The `mie` (*Machine Interrupt Enable*) register allows for a finer control of interrupts, allowing the programmer to set which types of interrupts are enabled: field `MSIE` (*Machine Software Interrupt Enable*), `MTIE` (*Machine Timer Interrupt Enable*), and `MEIE` (*Machine External Interrupt Enable*) control software, timer, and external interrupts, respectively.

The `mip` (*Machine Interrupt Pending*) register indicates the interrupts that are currently pending. Similarly to register `mie`, it specifies the type of interrupt on specific fields: `MSIP` (*Machine Software Interrupt Pending*), `MTIP` (*Machine Timer Interrupt Pending*), and `MEIP` (*Machine External Interrupt Pending*). Each of these fields may be writable or may be read-only. Register `mcause` (*Machine Cause*) provides information about the event that caused the trap. This register contains a field `I` specifying if the cause was an interrupt or an exception, while the rest of the bits are reserved for the exception code. RISC-V defines some of these exception codes, while others are left for the implementation to use.

Register `mtvec` (*Machine Trap-Vector Base-Address*) holds the trap vector configuration. Depending on the value of the `MODE` field, RISC-V allows for polled interrupts (*direct mode*, with a value of 0) or vectored interrupts (*vectored mode*, with a value of 1).

In direct mode, all traps cause the PC to be set to the address in the `BASE` field, while on vectored mode, traps set the PC to address $BASE + 4 \times cause$, `cause` being the exception code found in `mcause`. Finally, register `mepc` (*Machine Exception Program Counter*) holds the address of the instruction that generated the exception while it is handled.

When a trap is taken to M-mode, the corresponding flag in `mip` is set, and the `MIE` field in `mstatus` and the corresponding flag in `mie` are checked to determine if that interrupt is enabled. If it's enabled, the `MIE` field is copied into the `MPIE` field of `mstatus` and `MIE` is cleared, disabling further interrupts. Then, the previous privilege mode is stored in the `MPP` field of `mstatus`, the cause of the exception is encoded into `mcause`, the current PC is stored into the `mepc` register, and the PC is set to the address specified by `mtvec`. When the interrupt handler finishes, it calls `mret`, which resets the privilege mode (reading the `MPP` field in `mstatus`), re-enables interrupts (by copying back field `MPIE` to `MIE` in `mstatus`), and sets the PC to the value of `mepc`.

With regard to the `mip` register, the ISA states that if the field is writable, a pending interrupt can be cleared by clearing the field, but if the field is read-only, the implementation must provide some other mechanism for clearing the pending interrupt.

More details are available at the Master Thesis “Implementing Interrupts, Timers, and Memory-Mapped I/O in CREATOR” by Luis Daniel Casais Mezquida, and the RISC-V’s Specification.

MIPS architecture

Overview

CREATOR has a 32-bits build-in specification of the MIPS32 instruction set. A quick reference guide of this specification is available at: <https://creatorsim.github.io/creator/guides/mips32.pdf>.

MIPS 32 Reference Guide (CREATOR Simulator)

Registers

Name	Number	Use
zero	0	Constant 0
ra	1	Reserved for assembler
v0	2	Evaluation of expressions and function results
v1	3	Evaluation of expressions and function results
a0	4	Argument 1
a1	5	Argument 2
a2	6	Argument 3
a3	7	Argument 4
t0-t7	8-15	Temporal (no value is saved between calls)
t8-t9	16-23	Temporal (value is saved between calls)
t10-t11	24-25	Temporal (no value is saved between calls)
k0, k1	26, 27	Reserved for the operating system kernel
gp	28	Pointer to the global area
sp	29	Stack pointer
fp	30	Stack frame pointer
ra	31	Return address, used by function calls

System calls

Service	Call code	Arguments	Results
print_integer	\$a0 = 1	\$a0 = integer	
print_float	\$a0 = 2	\$f12 = real (32 bits)	
print_double	\$a0 = 3	\$f12 = real (64 bits)	
print_string	\$a0 = 4	\$a0 = string	Integer (\$v0)
read_integer	\$a0 = 5	\$a0 = integer	Real (32-bits (\$f0))
read_float	\$a0 = 6		Real (64-bits (\$f0))
read_double	\$a0 = 7	\$a0 = buffer, \$a1 = length	
read_string	\$a0 = 8	\$a0 = 9 \$a1 = quantity	Address (\$a0)
wait	\$a0 = 9	\$a0 = quantity	
putc	\$a0 = 10		
print_char	\$a0 = 11	\$a0 = byte	
read_char	\$a0 = 12		\$v0 (ASCII code)

Assembly directives

.data	The following data definitions that appear are stored in the data segment. It can include an argument that indicates the address from where the data will begin to be stored.
.text	The instructions that follow this directive are placed in the code segment. It can include a parameter that indicates where the code zone begins.
.global symbol	Declares a global symbol that can be referenced from other programs.
.extern label n	Declares that data stored from label occupies N bytes and that label is a global symbol. This directive allows the assembler to store data in an area of the data segment that can be accessed through the \$gp register.
.ascii string	Store the string in memory, but it does not end with NULL ('0')
.asciz string	Store the string in memory and place a NULL ('0') at the end.
.byte b1, ..., bn	Stores N values in successive bytes of memory.
.half h1, ..., hn	Stores N 16-bit numbers in consecutive half-words.
.word w1, ..., wn	Stores N 32-bit elements (words) in consecutive memory locations.
.float f1, ..., fn	Stores N real values of simple precision in consecutive memory positions.
.double d1, ..., dn	Stores N real double precision values in consecutive memory addresses.

Constant Handling Instructions

li Rdest, immediate	Load immediate value
lui Rdest, immediate	Load the 16 bits of the lower part of the immediate value in the upper part of the register. The bits of the lower part are set to 0.

Data transfer instructions

move Rdest, Rsrc	Move the contents of the Rsrc register to the Rdest register.
mfiio Rdest	Move the contents of the HI register to the Rdest register.
mfio Rdest	Move the contents of the LO register to the Rdest register.
mtb Rsrc	Move the contents of the Rsrc register to the HI register.
mtlo Rsrc	Move the contents of the Rsrc register to the LO register.

Load instructions

l Rdest, address	Load address in Rdest (the address value, not the content)
lb Rdest, address	Load the byte of the specified address and extend the sign
lbu Rdest, address	Load the byte of the specified address, do not extend the sign
lh Rdest, address	Load 16 bits of the specified address, sign is extended
lhu Rdest, address	Load 16 bits of the specified address, no sign is extended
lw Rdest, address	Load a word from the specified address.

Storing instructions

sb Rsrc, address	Stores the lowest Rsrc byte in the indicated address.
sh Rsrc, address	Stores the low half word (16 bits) of a register in the indicated memory address.
sw Rsrc, address	Store the Rsrc in the indicated address.



ARCOS-UC3M

MIPS 32 Reference Guide (CREATOR Simulator)

Arithmetic and logical instructions

In all the following instructions, Src2 can be both a register and an immediate value (a 16-bit integer) and in those where it puts imm it only accepts an immediate value

add Rdest, Rsrc1, Src2	Sum with overflow
addi Rdest, Rsrc1, imm	Add an immediate number with overflow
addu Rdest, Rsrc1, Src2	Sum without overflow
addiu Rdest, Rsrc1, imm	Add an immediate number without overflow
and Rdest, Rsrc1, Src2	AND logical operation
andi Rdest, Rsrc1, imm	AND logical operation with an immediate number
div Rdest, Rsrc1, Src2	Divide with overflow. Leave the quotient in the register lo and the rest in the register hi
divu Rdest, Rsrc1, Src2	Divide without overflow. Leave quotient in the register lo and the rest in the register hi
div Rdest, Rsrc1, Src2	Divide with overflow
divu Rdest, Rsrc1, Src2	Divide without overflow
mul Rdest, Rsrc1, Src2	Multiply without overflow
mult Rsrc1, Rsrc2	Multiply, the low part of the result is left in the lo register and the high part in the hi register
mult Rsrc1, Rsrc2	Multiply without overflow, the low part of the result goes to LO and the high part to HI
mod Rdest, Rsrc1, Rsrc2	Division module with overflow
modu Rdest, Rsrc1, Rsrc2	Division module without overflow
nop	It does not perform any operation
nor Rdest, Rsrc1, Src2	NOR Logic Operation
or Rdest, Rsrc1, Src2	OR Logic Operation
ori Rdest, Rsrc1, imm	OR Logic Operation with immediate
rem Rdest, Rsrc1, Rsrc2	Division module with overflow
rotl Rdest, Rsrc1, imm	Right rotation of Src2 number of bits
sl Rdest, Rsrc1, Src2	Logical bit shift to the left
srl Rdest, Rsrc1, Src2	Logical bit shift to the right
sra Rdest, Rsrc1, Src2	Arithmetic bit shift to the right
sub Rdest, Rsrc1, Src2	Subtraction (with overflow)
subu Rdest, Rsrc1, Src2	Subtraction (without overflow)
xor Rdest, Rsrc1, Src2	XOR Logic Operation

Branch and jump instructions

In all the following instructions, Src2 can be a register or an immediate value. Branch instructions use a signed 16-bit offset; So you can skip 215-1 instructions forward or 215 instructions backward. The jump instructions contain a 26-bit address field.

b label	Unconditional branch to the instruction that is on label.
beg Rsrc1, Src2, label	Conditional branch if Rsrc1 is equal to Src2.
bgez Rsrc, label	Conditional branch if the Rsrc register is equal to 0.
bge Rsrc1, Src2, label	Conditional branch if the Rsrc1 register is greater than or equal to Src2 (signed).
bgeu Rsrc1, Src2, label	Conditional branch if the Rsrc1 register is greater than or equal to Src2 (unsigned).
bgez Rsrc, label	Conditional branch if the Rsrc register is greater than or equal to 0.
bgeal Rsrc, label	Save the current address in the \$ra register (\$31)
blt Rsrc1, Src2, label	Conditional branch if the Rsrc1 register is greater than Src2 (signed).
bltu Rsrc1, Src2, label	Conditional branch if the Rsrc1 register is greater than Src2 (unsigned).
bltz Rsrc, label	Conditional branch if Rsrc is greater than 0.
blt Rsrc1, Src2, label	Conditional branch if Rsrc1 is less than or equal to Src2 (signed).
bltu Rsrc1, Src2, label	Conditional branch if Rsrc1 is less than or equal to Src2 (unsigned).
bltz Rsrc, label	Conditional branch if Rsrc is less than 0.
bltz Rsrc, label	Conditional branch if Rsrc is less than or equal to 0.
blt Rsrc1, Src2, label	Conditional branch if Rsrc1 is less than Src2 (signed).
bltu Rsrc1, Src2, label	Conditional branch if Rsrc1 is less than Src2 (unsigned).
bltz Rsrc, label	Conditional branch if Rsrc is less than 0.
bne Rsrc1, Src2, label	Conditional branch if Rsrc1 is not equal to Src2.
bnez Rsrc, label	Conditional branch if Rsrc is not equal to 0.
j label	Unconditional jump.
jal label	Unconditional jump, stores the current address at \$ra (\$31).
jalr Rsrc	Unconditional jump, stores the current address at \$ra (\$31).
jalr Rsrc1, Rsrc2	Unconditional jump, stores the current address in Rsrc1.
jr Rsrc	Unconditional jump.



ARCOS-UC3M

MIPS 32 Reference Guide (CREATOR Simulator)

Comparison instructions

In all the following instructions, Src2 can be both a register and an immediate value (a 16-bit integer).

seq Rdest, Rsrc1, Src2	Set Rdest to 1 if Rsrc1 is equal to Src2, 0 in other case.
sge Rdest, Rsrc1, Src2	Set Rdest to 1 if Rsrc1 is greater or equal to Src2, and 0 in other case (with sign).
sgtu Rdest, Rsrc1, Src2	Set Rdest to 1 if Rsrc1 is greater or equal to Src2, and 0 in other case (without sign).
set Rdest, Rsrc1, Src2	Set Rdest to 1 if Rsrc1 is greater than Src2, and 0 in other case (with sign).
setu Rdest, Rsrc1, Src2	Set Rdest to 1 if Rsrc1 is greater than Src2, y 0 in other case (without sign).
slt Rdest, Rsrc1, Src2	Set Rdest to 1 if Rsrc1 is little or equal to Src2, 0 in other case (with sign).
sltu Rdest, Rsrc1, Src2	Set Rdest to 1 if Rsrc1 is little or equal to Src2, 0 in other case (without sign).
slti Rdest, Rsrc1, Src2	Set Rdest to 1 if Rsrc1 is little than Src2, 0 in other case (with sign).
sltiu Rdest, Rsrc1, Src2	Set Rdest to 1 if Rsrc1 is little than Src2, 0 in other case (without sign).
sne Rdest, Rsrc1, Src2	Set Rdest to 1 if Rsrc1 not equal to Src2, and 0 in other case.

(Floating point) Constant Handling Instructions

l.f fd, value	Load the value (float) into the fs register of the mathematical coprocessor
l.d fd, value	Load the value (double) into the fd register of the mathematical coprocessor

(Floating point) Data transfer instructions

mfcc1 Rdest, CPsrc	Copy contents of the CPsrc register of the floating-point coprocessor to the Rdest CPU register.
mtcc1 Rsrc, CPdest	Copy contents of the Rsrc register of the CPU to the CPdest register of the floating-point coprocessor.
mov.s fd, fs	Move the contents of the fs record to the fd record. (float)
mov.d fd, fs	Move the contents of the fs record to the fd record. (double)

(Floating point) Arithmetic and logical instructions

In all the following instructions, Src2 can be both a register and an immediate value (a 16-bit integer) and in those where it puts imm it only accepts an immediate value

abs.s fd, fs	Absolute value of a real 32-bit number.
abs.d fd, fs	Absolute value of a real 64-bit number.
add.s fd, fs, ft	Add the register fs and ft and store the result in fd (float)
add.d fd, fs, ft	Add the register fs and ft and store the result in fd (double)
div.s fd, fs, ft	Divide fs by ft and leave the result in fd (float)
div.d fd, fs, ft	Divide fs by ft and leave the result in fd (double)
mul.s fd, fs, ft	Multiply the register fs and ft and leave your result in fd. (float)
mul.d fd, fs, ft	Multiply the register fs and ft and leave your result in fd. (double)
rsqrt.s fd, fs	Reciprocal Square Root (fd = 1.0/sqrt(fs)) (float)
rsqrt.d fd, fs	Reciprocal Square Root (fd = 1.0/sqrt(fs)) (double)
sqrt.s fd, fs	Square root of fs (float): fd=sqrt(fs)
sqrt.d fd, fs	Square root of fs (double)
sub.s fd, fs, ft	Subtraction (float): fd = fs-ft
sub.d fd, fs, ft	Subtraction (double)

(Floating point) Load instructions

l.s fs, address	Load in fs the value of the float (32 bits) found in the specified address.
l.d fd, address	Load fd with the value of double (64 bits) found in the specified address.

(Floating point) Store instructions

s.s fs, address	Stores the fs register in the indicated address. (float)
s.d fd, address	Store a double (64 bits) in the indicated address, the value of 64 bits comes from fd.

Conversion instructions

cv.t.s fd, fs	Turn a float into a double, the result is saved in fd
cv.t.w fd, Rsrc	Convert an integer to a double, the result is saved in fd
cv.t.d fd, fs	Turn a double into a float, the result is saved in fd
cv.t.w fd, Rsrc	Convert an integer into a float, the result is saved in fd
cv.t.w Rdest, fs	Convert a float into an integer, the result is saved in Rdest
cv.t.d Rdest, fs	Convert a double into an integer, the result is saved in Rdest



ARCOS-UC3M

System calls

The supported system calls are the following ones:

Service	Trap Code	Input	Output	Notes
print_int	\$v0 = 1	\$a0 = int to be printed	Print \$a0 to display	
print_float	\$v0 = 2	\$f12 = float to be printed	Print \$f12 to display	
print_double	\$v0 = 3	\$f12 = double to be printed	Print \$f12 to display	
print_string	\$v0 = 4	\$a0 = 1st char's address	Print string in standard output	
read_int	\$v0 = 5		Read integer to \$v0	
read_float	\$v0 = 6		Read float to \$v0	
read_double	\$v0 = 7		Read double to \$v0	
read_string	\$v0 = 8	\$a0 = buffer address, \$a1= buffer length	Read string	
sbrk	\$v0 = 9	\$a0 = number of bytes	\$v0 points to the allocated memory	Allocation from heap
exit	\$v0 = 10			End of execution

CLI User Guide

The CREATOR Command-Line Interface (CLI) provides a powerful text-based environment for assembly programming, debugging, and testing. It's designed for users who prefer working in a terminal and offers advanced features for development and automation.



Figure 1: CREATOR CLI interactive prompt.

The CLI version offers several key features:

- **Interactive Mode:** Full-featured REPL with command history
- **State Management:** Save and restore complete simulator snapshots
- **Configuration System:** Customize aliases, shortcuts, and preferences via YAML
- **Accessible Mode:** Screen reader support for visually impaired users

Installation

Installing CREATOR CLI

Installation via precompiled Binary

The easiest way to get started with the CLI version is to use the precompiled binaries. They include everything you need to run CREATOR without additional dependencies. Download the latest precompiled binary for your OS from the releases page and place it in a directory included in your

system's PATH as `creator-cli`.

You're all set! You can verify the installation by running:

```
1 creator-cli --help
```

To access the CLI from any terminal, ensure the binary is in your PATH or create a symbolic link to it in a directory that is. See below for instructions on creating an alias.

Building from Source

Alternatively, you can build the CREATOR CLI locally.

Prerequisites

- Git is required to download the project.
- Deno must be installed on your system. Follow the instructions on the Deno website to install it.
- Bun is the recommended package manager to install dependencies.

Steps

1. Clone the CREATOR repository:

```
1 git clone https://github.com/creatorsim/creator-beta.git --recurse-submodules --  
   depth=1  
2 cd creator-beta  
3
```

2. Install dependencies:

```
1 bun install  
2
```

3. Build the CLI:

```
1 bun build:cli  
2
```



This build script **requires** having Bun installed, but if you don't want to, you can use another package manager (e.g., NPM) and do:

```
npm wasm:cli && npm build:cli:native
```

4. Test your installation:

```
1 creator-cli --help  
2
```

You should see the CREATOR help message with available options.



You can also just run the CLI without building with Deno:

```
deno run --allow-all src/cli/creator6.mts --help
```

Getting Architecture Files

CREATOR requires architecture definition files to simulate different processors. These files are in YAML format and define the instruction set, registers, memory layout, and other architecture-specific details.

Default Architectures

The repository includes several architecture files in the `architecture/` directory. The releases also include an `architectures.zip` file with the same contents.

For example, the following architectures are provided:

- `RV32IMFD.yml` - RISC-V 32-bit
- `RV64IMFD.yml` - RISC-V 64-bit
- `MIPS32.yml` - MIPS 32-bit
- `Z80.yml` - Z80 8-bit processor (with interrupts)

Configuration

The CLI version supports user configuration via a YAML file located at:

- **macOS/Linux:** `~/.config/creator/config.yml`
- **Windows:** `%USERPROFILE%\config\creator\config.yml`

This file is automatically created with defaults on first run. See the Configuration section for more details.

Updating

If you installed via precompiled binaries, download the latest version from the releases page.

To update the CLI version, pull the latest changes from the repository and reinstall dependencies:

```
git pull origin main && bun install
```

Command-Line Options

The CREATOR CLI accepts various command-line options to configure architecture, input files, and behavior.

Basic Usage

```
1 creator-cli [options]
```

Required Options

--architecture, -a

Required: Yes

Type: String (path to YAML file)

Description: Path to the architecture definition file. Specifies which processor architecture to simulate.

Examples:

```
1 : RISC-V architecture
2 creator-cli --architecture architecture/riscv32.yml --assembly program.s
3 : MIPS architecture
4 creator-cli --architecture architecture/mips32.yml -s program.s
```

Input Options

--assembly, -s

Type: String (path to assembly file)

Description: Assembly source file to assemble and load. Assembles the specified file and loads it into memory. **Example:**

```
1 creator-cli -a architecture/riscv32.yml --assembly hello.s
```

--bin, -b

Type: String (path to binary file)

Description: Binary file to load directly into memory. Loads a pre-assembled binary file without compilation. **Example:**

```
1 creator-cli -a architecture/riscv32.yml --bin programlbin
```

Note: Binary and assembly options are mutually exclusive. If both are provided, binary takes precedence.

`--library, -l`

Type: String (path to library file)

Description: Library file to load before assembly. Loads a library of pre-assembled code that your program can reference. This is only supported when using the default CREATOR assembler. **Example:**

```
1 creator-cli -a architecture/riscv32.yml -l stdlib.yml -s program.s
```

Assembler Options

`--assembler, -C`

Type: String

Default: default

Description: Assembler backend to use. Selects which assembler to use for compilation.

Available Options:

- default - CREATOR native assembler
- sjasmplus - Z80 assembler with macro support
- rasm - Alternative Z80 assembler

Examples:

```
1 : Use default CREATOR assembler
2 creator-cli -a architecture/riscv32.yml -s program.s
3
4 : Use sjasmplus for Z80
5 creator-cli -a architecture/z80.yml -s program.s --assembler sjasmplus
6
7 : Use rasm for Z80
8 creator-cli -a architecture/z80.yml -s program.s -C rasm
9
```

`--isa, -i`

Type: Array of strings

Default: []

Description: ISA extensions to load. In supported architectures, specifies which ISA extensions to enable. If unspecified, the full ISA defined in the architecture file is used.

Examples:

```
1 : RISC-V with M extension (multiply/divide)
2 creator-cli -a architecture/riscv32.yml --isa M -s program.s
3
4 : RISC-V with multiple extensions
```

```
5 creator-cli -a architecture/riscv32.yml --isa M F D -s program.s
6
7 : RISC-V base only (no extensions)
8 creator-cli -a architecture/riscv32.yml -s program.s
9
```

Other Options

--accessible, -A

Type: Boolean

Default: false

Description: Enable accessible mode for screen readers. Disables colors, ASCII art, and fancy formatting for compatibility with screen readers.

Example:

```
1 creator-cli --accessible -a riscv32.yml -s program.s
```

Changes in Accessible Mode:

- - No ANSI color codes
- - Plain text output only
- - No ASCII art
- - Descriptive text for all information
- - Structured table layouts

Note: Can also be set in configuration file. Command-line flag overrides config.

--config, -c

Type: String (path to YAML file)

Default: ~/.config/creator/config.yml

Description: Path to configuration file. Specifies a custom configuration file instead of the default location.

Example:

```
1 creator-cli -a riscv32.yml -s program.s --config custom-config.yml
```

See Configuration for config file format.

--state**Type:** String (path to JSON file)**Default:** None**Description:** File to save execution state on exit. Saves the current simulator state to the specified file.**Example:**

```
1 creator-cli -a riscv32.yml -s program.s --state mystate.json
```

Note: Use `restore` command in interactive mode to load saved states.**--reference, -r****Type:** String (path to file)**Default:** None**Description:** Reference file for validation. Used for grading and validation of student exercises. Not typically used by end users. See Grading Student Exercises for details.**--interrupt-handler****Possible values:** "default", "custom"**Default:** "default"**Description:** Interrupt handler to use, either CREATOR's default handler or a custom architecture-defined one. Selects the desired interrupt handler to use: CREATOR's default handler, with support for architecture-defined system calls, or a fully custom architecture-defined one.**Example:**

```
1 creator-cli -a riscv32.yml -s program.s --interrupt-handler custom
```

See Interrupt Support for a guide on how to use these features.

Getting Help

Show all available options:

```
1 creator-cli --help
```

Commands Reference

Complete reference for all CREATOR CLI commands. Commands are case-insensitive and support aliases defined in your configuration.

Execution Control

step

Execute one instruction and display the result.

Syntax: `step` or just press Enter. **Alias:** Configured in config file (commonly `s`)

Output:

```
1 0x00400000 (0x00000293) addi t0,zero,0
```

Shows: `<address>` (`<machine_code>`) `<assembly>`

Behavior:

- Executes the instruction at current PC
- PC advances to next instruction - Registers and memory update accordingly
- State is saved for `unstep`

When to Use:

- Step-by-step debugging
 - Observe instruction-level behavior
 - Verify each operation
-

unstep

Undo the last executed instruction (reverse step).

Syntax: `unstep`

Alias: Configured in config file

Requirements:

- `max_states` must be set in config (`>0`)
- At least one instruction must have been executed

Behavior:

- Restores simulator to state before last instruction
- PC moves backward

- Register and memory changes reverted
- Can unstep multiple times up to `max_states` limit

Example:

```

1 CREATOR> step
2 0x00400000 (0x00000293) addi t0,zero,0
3
4 CREATOR> unstep
5 # PC back at 0x00400000, t0 unchanged

```

When to Use:

- Went too far in debugging
 - Want to re-examine instruction
 - Study before/after states
-

run [count]

Execute multiple instructions continuously.

Syntax:

- `run` - Run until completion or breakpoint
- `run <count>` - Run exactly N instructions

Alias: Configured in configuration file (commonly `r`)

Examples:

```

1 CREATOR> run           # Run to completion
2 CREATOR> run 100      # Run 100 instructions
3 CREATOR> run 1000000  # Run 1 million instructions

```

Stops When: - Program completes (`execution_index = -2`) - Breakpoint is hit - Error occurs - Pause shortcut issued

Output:

- Each instruction displayed as it executes
- “Program execution completed.” when done
- “Breakpoint hit at” when breakpoint reached

Performance:

- Executes in chunks for responsive UI
 - Can pause mid-execution
-

`silent [count]`

Run instructions without displaying output.

Syntax:

- `silent` - Run silently until completion
- `silent <count>` - Run N instructions silently

Use Cases:

- Fast execution without visual clutter
- Performance testing
- Running initialization code
- Getting to a specific point quickly

Example:

```
1 CREATOR> silent 1000 # Skip first 1000 instructions
2 CREATOR> list # Now see where we are
```

`continue`

Resume execution from paused or stepped state.

Syntax: `continue`

Alias: Configured in config file (commonly `c`)

Behavior:

- If paused mid-run: Resumes from current point
- If at breakpoint: Steps once then continues running
- Otherwise: Steps once then runs

Example Flow:

```

1 CREATOR> run
2 # ... executes many instructions ...
3 CREATOR> pause
4 Execution paused.
5
6 CREATOR> continue
7 # Resumes execution

```

nur

uN-Run (reverse run) - Step backwards until breakpoint or program start.

Syntax: nur

Requirements:

- `max_states` must be set in config
- Sufficient state history available

Behavior:

- Repeatedly unsteps
- Stops at breakpoints (going backwards)
- Stops when no more history available

Example:

```

1 CREATOR> run          # Execute past several breakpoints
2 CREATOR> nur         # Go back to last breakpoint

```

When to Use:

- Overshot target during debugging
 - Want to re-examine earlier state
 - Find when something changed
-

until <address|label>

Run until specified address is reached.

Syntax: until <address> or until <label>

Examples:

```
1 CREATOR> until 0x400010 # Run until address
2 CREATOR> until loop_end # Run until label
```

Behavior:

1. Sets temporary breakpoint at address/label
2. Runs program
3. When breakpoint hit, removes it

Equivalent To:

```
1 break <address>
2 run
3 break <address> # Toggle off
```

reset

Reset simulator to initial state.

Syntax: reset

What Gets Reset:

- Program counter to entry point
- All registers to initial values
- Memory to loaded state (ROM + initialized data)
- Execution history cleared
- All temporary state cleared

What Persists:

- Loaded program
- Architecture definition
- Breakpoints (optional: can clear manually)

Example:

```
1 CREATOR> run
2 Program execution completed.
3
4 CREATOR> reset
```

```

5 Program reset.
6
7 CREATOR> list
8 # Back at start

```

Breakpoint Management

break [address|label]

Set, remove, or list breakpoints.

Syntax:

- **break** - List all breakpoints
- **break** <address> - Toggle breakpoint at hex address
- **break** <label> - Toggle breakpoint at label
- **break** <hex_number> - Toggle at hex (without 0x)

Alias: Commonly **b**

Examples:

```

1 CREATOR> break # List breakpoints
2 CREATOR> break 0x400008 # Toggle at address
3 CREATOR> break main # Toggle at label
4 CREATOR> break 10 # Toggle at address 0x10

```

Output:

```

1 Breakpoint set at 0x00400008 (loop): addi t0,t0,1
2 # or
3 Breakpoint removed at 0x00400008 (loop): addi t0,t0,1

```

Label Resolution: - If input matches a label, uses label's address - Otherwise, treats as hex address (with or without 0x prefix)

Visual Indicators:

- - Red * in list output
 - - Red highlighting of instruction line
 - - Mentioned in breakpoint list
-

Inspection Commands

`list [limit]`

Display loaded instructions with addresses, labels, and code.

Syntax:

- `list` - Show all instructions
- `list <n>` - Show first N instructions
- `list --limit <n>` - Show first N instructions (explicit)

Output Format (When loading an Assembly Source):

```

1  B | Address | Label   | Loaded Instruction | User Instruction
2  ---|-----|-----|-----|-----
3  > | 0x400000| main   | addi t0,zero,0x123 | li t0, 0x123
4  | 0x400004|       | lui a0,0x10000    | la a0, myword

```

Output Format (When loading a Binary File):

```

1  B | Address | Label   | Decoded Instruction | Machine Code (hex)
2  ---|-----|-----|-----|-----
3  > | 0x400000| main   | addi t0,zero,0x123 | 0x12300293

```

Columns:

- **B**: Breakpoint indicator (* if set)
- **>**: Current PC indicator (green)
- **Address**: Instruction memory address
- **Label**: Label at this address (if any)
- **Loaded/Decoded**: The actual instruction in memory
- **User/Machine**: Original source or machine code hex

Colors (in normal mode):

- Green: Current instruction (at PC)
 - Yellow: Previously executed instruction
 - Red: Instructions with breakpoints
-

insn

Display the current instruction at PC.

Syntax: `insn`

Output:

```
1 0x00400000 (0x00000293) addi t0,zero,0x123
```

Shows the instruction about to be executed.

reg <registerBank|name> [format]

Display register values.

Syntax:

- `reg list` - List available register banks
- `reg <registerBank>` - Show all registers of register bank
- `reg <registerBank> <format>` - Show registers in specific format
- `reg <name>` - Show specific register
- `reg <name> <format>` - Show specific register in format

Formats:

- `- raw` - Hexadecimal (default)
- `- decimal` or `dec` - Decimal (signed)
- `- number` - Same as decimal

Examples:

```
1 CREATOR> reg list
2 Register types:
3   int_registers
4   fp_registers
5
6 CREATOR> reg int_registers
7 int_registers:
8 zero(x0): 0x00000000  ra(x1): 0x00000000  sp(x2): 0x7FFFFFFC  gp(x3): 0x10008000
9 t0(x5):  0x00000123  t1(x6): 0x00000000  t2(x7): 0x00000000  fp(x8): 0x00000000
10 ...
11
12 CREATOR> reg int_registers dec
```

```

13 int_registers:
14 zero(x0): 0      ra(x1): 0      sp(x2): 2147483644  gp(x3): 268468224
15 t0(x5): 291     t1(x6): 0      t2(x7): 0      fp(x8): 0
16 ...
17
18 CREATOR> reg t0
19 t0: 0x00000123 | 291
20
21 CREATOR> reg pc
22 PC: 0x00400000 | 4194304

```

mem <address> [count]

Display memory contents with hints and annotations.

Syntax:

- - mem <address> - Show one word at address
- - mem <address> <count> - Show count bytes starting at address

Address Format:

- - Hexadecimal with 0x prefix: 0x10000000
- - Hexadecimal without prefix: 10000000

Examples:

```

1 CREATOR> mem 0x10000000
2 0x10000000: 0x12345678
3
4 CREATOR> mem 0x10000000 16
5 0x10000000: 0x12345678 // myvar:int (32b)
6 0x10000004: 0x00000064 // count:int (32b)
7 0x10000008: 0x00000001
8 0x1000000C: 0x00000002

```

Features:

- - **Hints:** Shows variable names and types if available
- - **Colors** (normal mode): Different colors for different hints
- - **Word-aligned:** Displays in architecture word sizes
- - **Annotations:** Comments show semantic information

Hints Format:

```
1 0x10000000: 0x12345678 // tag:type (size in bits) @+offset
```

Multiple Hints Per Word:

```
1 0x10000000: 0x12FF00AB // a:char (8b) @+0, b:char (8b) @+1, c:short (16b) @+2
```

Each hint is color-coded differently.

hexview <address> [count] [bytes_per_line]

Display memory in hexdump format with ASCII representation.

Syntax:

- - hexview <address> - Default: 16 bytes, 16 per line
- - hexview <address> <count> - Specified bytes, 16 per line
- - hexview <address> <count> <bytes_per_line> - Custom layout

Examples:

```
1 CREATOR> hexview 0x10000000
2 0x10000000: 78 56 34 12 48 65 6C 6C 6F 20 57 6F 72 6C 64 00 |xV4.Hello World.|
3
4 CREATOR> hexview 0x10000000 32 8
5 0x10000000: 78 56 34 12 48 65 6C 6C |xV4.Hell|
6 0x10000008: 6F 20 57 6F 72 6C 64 00 |o World.|
7 0x10000010: 00 00 00 00 00 00 00 00 |.....|
8 0x10000018: 00 00 00 00 00 00 00 00 |.....|
```

Format:

```
1 <address>: <hex bytes...> |<ASCII>|
```

ASCII Column:

- - Printable characters shown as-is
- - Non-printable shown as . - Useful for finding strings in memory

stack [max_bytes]

Display call stack information and stack memory contents.

Syntax:

- - `stack` - Show stack with default limit (256 bytes)
- - `stack <max_bytes>` - Show up to specified bytes

Output Sections:

1. Call Stack Hierarchy:

```

1 Call Stack:
2   > main (0x7FFFFFFC - 0x7FFFFFF0, 12 bytes)
3     * calculate (0x7FFFFFF0 - 0x7FFFFE4, 12 bytes)
4       * helper (0x7FFFFE4 - 0x7FFFFDC, 8 bytes)

```

2. Current Frame Details:

```

1 Current Frame Details:
2 Function: helper
3 Frame: 0x7FFFFE4 - 0x7FFFFDC
4 Size: 8 bytes
5 Caller: calculate
6 Caller frame: 0x7FFFFFF0 - 0x7FFFFE4

```

3. Stack Memory Contents:

```

1 Stack Memory Contents:
2 0x7FFFFDC: 0x00000000 ← SP, helper frame start
3 0x7FFFFE0: 0x00400020 // return address
4 0x7FFFFE4: 0x00000005 ← helper frame end, calculate frame start
5 0x7FFFFE8: 0x00400010 // saved ra
6 0x7FFFFEC: 0x00000003 // local_var
7 0x7FFFFFF0: 0x00400000 ← calculate frame end, main frame start

```

Frame Colors (normal mode):

- - Each stack frame shown in different color
- - Current (top) frame in green
- - Older frames in cyan, magenta, blue, yellow

Annotations:

- - Frame boundaries marked
 - - Stack pointer (SP) indicated
 - - Variable names from hints
 - - Return addresses identified
-

State Management

snapshot [filename]

Save complete simulator state to a JSON file.

Syntax:

- - `snapshot` - Auto-generate timestamped filename
- - `snapshot <filename>` - Save to specific file

Auto-Generated Format:

```
1 snapshot-2025-01-15T10-30-45-123Z.json
```

Saved State Includes:

- - All register values
- - All memory contents
- - Program counter
- - Execution state
- - Previous PC (for display)
- - Stack tracker state
- - Custom extra data

Example:

```
1 CREATOR> run 100
2 CREATOR> snapshot debug-state.json
3 Snapshot saved to debug-state.json
4
5 CREATOR> run
6 Program execution completed.
7
8 CREATOR> restore debug-state.json
9 State restored from debug-state.json
10
11 CREATOR> list
12 # Back at instruction 100
```

Use Cases:

- - Save progress before risky operations
- - Create checkpoints during debugging

- - Share reproducer for bugs
 - - Test different execution paths from same state
-

restore <filename>

Restore simulator state from a snapshot file.

Syntax: restore <filename>

Requirements: - File must be valid snapshot JSON - Architecture must match

Behavior:

1. Resets current state
2. Loads snapshot from file
3. Restores all registers, memory, PC
4. Restores previous PC tracking
5. Ready to continue from restored point

Example:

```
1 CREATOR> restore checkpoint1.json
2 State restored from checkpoint1.json
3
4 CREATOR> reg pc
5 PC: 0x00400064 | 4194404
6
7 CREATOR> step
8 # Continue from restored state
```

Utility Commands

clear

Clear the terminal screen.

Syntax: clear

Effect: - Clears all terminal output - Prompt reappears at top - State unchanged

When to Use:

- - Declutter after lots of output
 - - Fresh view for new debugging session
 - - Before taking screenshot
-

help

Display all available commands with brief descriptions.

Syntax: help

Output:

- List of all commands
 - Brief description of each
 - Keyboard shortcuts (if enabled)
 - Aliases (from configuration)
-

about

Display information about CREATOR.

Syntax: about

Shows:

- CREATOR version
 - CLI version
 - Runtime version (Deno/Node)
 - Platform information
 - Copyright and credits
-

alias

List defined command aliases.

Syntax: alias

Output:

```
1 Current command aliases:
2 s → step
3 b → break
4 r → run
5 c → continue
6 reg → reg int_registers
```

Aliases can be defined in your config file at: `/.config/creator/config.yml`

Note: Aliases are defined in Configuration file, not via command.

quit

Exit the simulator.

Syntax: quit

Behavior:

- Exits interactive mode
- Closes the simulator
- No confirmation prompt

Data Loss Warning:

- Unsaved state is lost
 - Use `snapshot` before quitting to save progress
-

Command Aliases

Commands support aliasing via configuration file.

Common aliases are:

- `s → step`

- `b` → `break`
- `r` → `run`
- `c` → `continue`
- `u` → `unstep`

See Configuration for setting up aliases.

Keyboard Shortcuts

When `keyboard_shortcuts` is enabled in config, single key-presses can execute commands:

- `Ctrl+S` → `step` (example)
- `Ctrl+B` → `break` (example)
- `Ctrl+L` → `clear` (example)

See Configuration for setting up shortcuts.

Configuration

CREATOR supports extensive configuration through YAML files, allowing you to customize behavior, create command aliases, and define keyboard shortcuts.

Configuration File Location

Default location: `~/.config/creator/config.yml`

Custom location: Use `--config` option:

```
1 creator-cli --config ~/my-creator-config.yml program.s
```

If the configuration file doesn't exist, CREATOR creates it with default settings automatically.

Configuration Structure

The configuration file has three main sections:

```
1 settings :  
2   # General behavior settings  
3 aliases :
```

```
4 # Command aliases (shortcuts for long commands)
5 shortcuts:
6 # Single-key keyboard shortcuts
```

Settings Section

Available Settings

max_states (number):

- - Maximum number of states saved for `unstep/nur` (reverse execution)
- - 0: Reverse execution disabled
- - -1: Unlimited history (uses more memory)
- - Default: 100

accessible (boolean):

- - Enable accessibility mode for screen readers - Provides verbose, structured output
- - Disables visual formatting
- - Default: `false`

keyboard_shortcuts (boolean):

- - Enable single-key shortcuts in interactive mode
- - Default: `true`

auto_list_after_shortcuts (boolean):

- - Automatically run `list` command after keyboard shortcuts
- - Helps see context after stepping
- - Default: `true`

Example Settings

```
1 settings:
2   max_states: 50 # Keep last 50 states
3   accessible: false # Standard visual mode
4   keyboard_shortcuts: true # Enable shortcuts
5   auto_list_after_shortcuts: false # Manual listing
```

Aliases Section

Create command shortcuts to save typing.

Syntax

```
1 aliases :
2   alias_name: full_command
```

Built-in Examples

```
1 aliases :
2   # Short names for common commands
3   s: step
4   r: run
5   b: break
6
7   # Register groups
8   regs: reg int_registers
9   fregs: reg fp_registers
10
11  # Common inspections
12  pc: reg pc
13  sp: reg sp
14  ra: reg ra
15
16  # Memory dumps
17  text: hexview 0x00400000 64 16
18  data: hexview 0x10010000 64 16
19  stack: mem sp 16
```

Custom Aliases

You can create aliases for any command with arguments:

```
1 aliases :
2   # Debugging helpers
3   showargs: reg a0 a1 a2 a3
4   showtemps: reg t0 t1 t2 t3 t4 t5 t6
5
6   # Quick breakpoints
7   bmain: break main
```

```

8  bloop: break main_loop
9
10 # Memory views with hints
11  datahint: mem 0x10010000 8 —hints
12
13 # Step multiple times
14  step5: step 5
15  step10: step 10
16
17 # Combined operations
18  runshow: run; reg; stack

```

Using Aliases

Once defined, use them like regular commands:

```

1 creator> s          # Same as 'step'
2 creator> showargs # Same as 'reg a0 a1 a2 a3'
3 creator> datahint # Same as 'mem 0x10010000 8 --hints'

```

Shortcuts Section

Define single-key shortcuts for interactive mode.

Syntax

```

1 shortcuts:
2   command: "key"

```

The key must be a single character (in quotes).

Default Shortcuts

```

1 shortcuts:
2   step: " " # Spacebar
3   run: "r"
4   break: "b"
5   snapshot: "s"
6   unstep: "u"
7   quit: "q"
8   help: "h"
9   list: "l"

```

Custom Shortcuts

```
1 shortcuts:
2   # Execution control
3   step: " " # Spacebar
4   run: "r"
5   continue: "c"
6   reset: "x"
7
8   # State inspection
9   reg: "g" # 'g' for reGisters
10  mem: "m"
11  stack: "k"
12
13  # Debugging
14  break: "b"
15  list: "l"
16  unstep: "u"
17  snapshot: "s"
18  restore: "o" # 'o' for lOad
19
20  # Utility
21  help: "h"
22  clear: "z"
23  quit: "q"
```

Shortcut Behavior

- Press the key once to execute the command.
- If `auto_list_after_shortcuts` is enabled, instructions list automatically.
- Shortcuts work only in interactive mode.
- Disable with `keyboard_shortcuts: false`.

Complete Example Configuration

```
1 # ~/.config/creator/config.yml
2
3 settings:
4   max_states: 50
5   accessible: false
6   keyboard_shortcuts: true
7   auto_list_after_shortcuts: true
```

```
8
9 aliases:
10 # Basic command shortcuts
11 s: step
12 r: run
13 b: break
14 c: continue
15 # Register shortcuts
16 pc: reg pc
17 sp: reg sp
18 ra: reg ra
19 args: reg a0 a1 a2 a3 a4 a5 a6 a7
20 temps: reg t0 t1 t2 t3 t4 t5 t6
21 saved: reg s0 s1 s2 s3 s4 s5 s6 s7 s8 s9 s10 s11
22
23 # Memory shortcuts
24 text: hexview 0x00400000 64 16
25 data: hexview 0x10010000 64 16
26 stackview: mem sp 16
27 stackhex: hexview sp 64 16
28
29 # Debugging shortcuts
30 here: insn
31 where: reg pc
32 showstate: reg; stack
33
34 # Quick stepping
35 s5: step 5
36 s10: step 10
37 u5: unstep 5
38
39 shortcuts:
40 step: " "
41 run: "r"
42 break: "b"
43 snapshot: "s"
44 unstep: "u"
45 quit: "q"
46 help: "h"
47 list: "l"
48 clear: "z"
```

Configuration Loading

CREATOR loads configuration in this order:

1. **Default config:** Built-in settings
2. **User config:** `~/.config/creator/config.yml` (if exists)
3. **Custom config:** `--config` option (if specified)
4. **Command-line options:** Override config file settings

Teaching Resources

CREATOR is a powerful tool for teaching computer architecture and assembly programming. This document provides resources and guidance for educators looking to integrate CREATOR into their curriculum.

CREATOR's CLI also allows you to validate a program against an expected final state. This includes specifying the values of memory, registers (including floating point registers, within an error threshold), and the display buffer, and whether to error on calling convention errors (sentinel). See [Validating Program Execution](#) for more information.

CREATOR allows educators to create custom architectures tailored to their curriculum. This can be done by defining new architecture YAML files that specify instruction sets, registers, memory layout, and other architecture-specific details. See ["Creating Custom Architectures"](#) for more information.

Setting up the Remote Laboratory

The remote laboratory allows users to remotely execute their programs on real hardware through the use of multiple CREATOR Gateways.



Currently, only the ESP32 Gateway is supported.

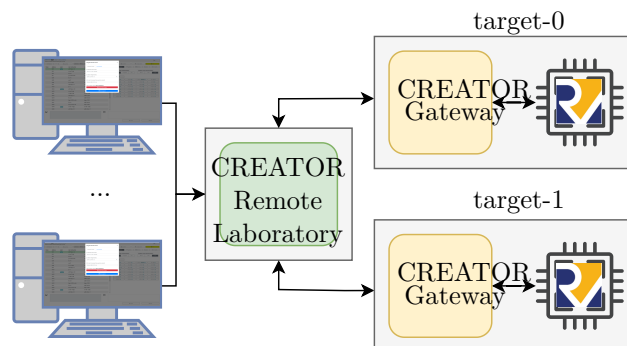


Figure 2: CREATOR Remote Laboratory diagram.

Setup and configuration

The recommended way of running the remote laboratory is through the Docker image.



For alternative ways of execution, check the source repository.

First, create a file structure such as this:

```
creator-remote-lab/
+-- compose.yaml
+-- results/
+-- config/
|  +-- deployment.json
```

On the remote lab container configuration: - `results/` must be mounted to `/app/results/` and `config/` to `/app/config/` - The server will listen on port 5000, so we should expose that port - In order to send the results via email, you must set your Google Mail address in the `EMAIL` environment variable and your app password in the `PASSW` environment variable.

We should also deploy the gateways. More information on CREATOR Gateway.

We can do all this with Docker Compose, in the `compose.yaml` file:

```
1 services:
2   creator-remote-lab:
3     image: creatorsim/creator-remote-lab:latest
4     volumes:
5       - ./config:/app/config
6       - ./results:/app/results
7     ports:
8       - "5000:5000"
9     environment:
10      - EMAIL=test@arcos.inf.uc3m.es # google mail address
11      - PASSW=abcdefghijklmnop # google app password
12
13 target-0:
14   image: creatorsim/creator-gateway-esp32:latest
15   devices:
16     - /dev/ttyUSB0
17   stdin_open: true
18   tty: true
19
20 target-1:
21   image: creatorsim/creator-gateway-esp32:latest
22   devices:
23     - /dev/ttyUSB1
24   stdin_open: true
25   tty: true
```

The configuration of the target boards is placed in `config/deployment.json`. You must provide the type of board (`target_board`), the USB port of the board (`target_port`), and the URL of the

gateway server (`target_url`). As we're doing everything with Docker Compose, we can just use their container names and prevent exposing the ports to `localhost`.

E.g.:

```

1 {
2   "target-0": {
3     "target_board": "esp32c3",
4     "target_port": "/dev/ttyUSB0",
5     "target_url": "http://target-0:8080"
6   },
7   "target-1": {
8     "target_board": "esp32c3",
9     "target_port": "/dev/ttyUSB1",
10    "target_url": "http://target-1:8080"
11  }
12 }
```

The execution results will be stored in the `results/` folder.

Then, we can deploy everything with:

```
1 docker compose up
```

CREATOR API (CAPI)

CAPI allows instruction definitions to interact with custom CREATOR functions.



CAPI is a global variable, so you can access it from your browser's developer console if you're using the web application.

Memory

Interaction with CREATOR's memory.

CAPI.MEM.write

```
CAPI.MEM.write(
  address: bigint,
  bytes: number,
  value: bigint,
  reg_name?: string,
  hint?: string,
```

```

    noSegFault: boolean = true,
  ): void { }

```

Writes a specific value to the specified address and number of bytes. You can provide extra information about which register used to hold the value (`reg_name`), or any hint about what that value might be (`hint`). To enable checking if the address is in a writable segment, set `noSegFault` to false.

E.g.:

```

CAPI.MEM.write(registers.t0, 1, registers.t0, "t0");

```

CAPI.MEM.read

```

CAPI.MEM.read(
  address: bigint,
  bytes: number,
  reg_name: string,
  noSegFault: boolean = true,
): bigint { }

```

Reads a specific number of bytes in the specified address and returns them. You can provide extra information about which register will hold the value (`reg_name`). To enable checking if the address is in a readable segment, set `noSegFault` to false.

E.g.:

```

registers.t0 = CAPI.MEM.read(registers.t1, 1, "t0");

```

CAPI.MEM.addHint

```

CAPI.MEM.addHint(address: bigint, hint: string, sizeInBits?: number): boolean { }

```

Adds a `hint` (description of what the address holds) for the specified memory `address`. If a hint already exists at the specified address, it replaces it. You can optionally specify the size of the stored type in bits (`sizeInBits`). Returns `true` if the hint was successfully added, else `false`.

E.g.:

```

CAPI.MEM.addHint(registers.f0, "float64", 64);

```

System calls

CREATOR's system calls.

CAPI.SYSCALL.exit

```
CAPI.SYSCALL.exit(): void { }
```

Terminates the execution of the program.

E.g.:

```
CAPI.SYSCALL.exit();
```

CAPI.SYSCALL.print

```
CAPI.SYSCALL.print(  
  value: number | bigint,  
  type: "int32" | "float" | "double" | "char" | "string",  
) : void { }
```

Prints the specified value of the specified type to the console.

Supported types are:

- - "int32": signed 32-bit integer
- - "float" / "double": JS's
- Number
- - "char": UTF-16 character value
- - "string": address of a null-terminated array of 1-byte chars

E.g.:

```
CAPI.SYSCALL.print(registers.a0, "char");
```

CAPI.SYSCALL.read

```
CAPI.SYSCALL.read(  
  dest_reg_info: string,  
  type: "int32" | "float" | "double" | "char" | "string",  
  aux_info?: string,  
) : void { }
```

Reads the specified value type from the console and stores it in the specified register by name (dest_reg_info).

Supported types are:

- - "int32": signed 32-bit integer
- - "float" / "double": JS's
- Number
- - "char": UTF-16 character value
- - "string": `aux_info` is the name of the register that holds the address of a null-terminated array of 1-byte chars

E.g.:

```
CAPI.SYSCALL.read("a0", "char");
CAPI.SYSCALL.read("a0", "string", "a1");
```

CAPI.SYSCALL.get_clk_cycles

```
CAPI.SYSCALL.get_clk_cycles(): number { }
```

Returns the number of clock cycles that have passed since the program started.

E.g.:

```
CAPI.SYSCALL.get_clk_cycles();
```

Validation

CAPI.SYSCALL.raise

```
CAPI.SYSCALL.raise(msg: string): never { }
```

Raises an error with a specific msg.

E.g.:

```
CAPI.SYSCALL.raise("Help!");
```

CAPI.SYSCALL.isOverflow

```
CAPI.SYSCALL.isOverflow(op1: bigint, op2: bigint, res_u: bigint): boolean { }
```

Checks if the result `res_u` of operating two operands `op1` and `op2` caused an overflow.

E.g.:

```
CAPI.SYSCALL.isOverflow(registers.t0, registers.t1, registers.t0 + registers.t1);
```

Stack

These functions are used for the stack tracker and sentinel modules, and are a way to tell CREATOR when a new function frame begins and ends. They should be included in the instructions that jump to, or return from, a routine, as is the case of RISC-V's `jal` and `jr` instructions.

CAPI.STACK.beginFrame

```
CAPI.STACK.beginFrame(addr?: bigint): void { }
```

Marks the beginning of a function frame at `address`. If not specified, it takes the current (real) value of the program counter.

E.g.:

```
registers.pc = ...
CAPI.SYSCALL.beginFrame();
```

CAPI.STACK.endFrame

```
CAPI.STACK.endFrame(): void { }
```

Ends the current stack frame.

E.g.:

```
registers.pc = ...
CAPI.SYSCALL.endFrame();
```

Floating point

CAPI.FP.split_double

```
CAPI.FP.split_double(reg: bigint, index: 0 | 1): string { }
```

Given a double precision IEEE 754 value `reg`, gets the 32-bits most significant (`index=1`) bits or the least significant bits (`index=0`). It returns it as a string of bits.

E.g.:

```
const foo = CAPI.FP.split_double(registers.t0, 1);
```

CAPI.FP.uint2float32

```
CAPI.FP.uint2float32(value: number): number { }
```

Transforms the unsigned integer `value` to a single precision IEEE754 JS Number.

E.g.:

```
CAPI.FP.uint2float32(5);
```

CAPI.FP.float322uint

```
CAPI.FP.float322uint(value: number): bigint { }
```

Transforms the single precision floating point (JS Number) `value` into an unsigned integer.

E.g.:

```
CAPI.FP.float322uint(5.0);
```

CAPI.FP.int2uint

```
CAPI.FP.int2uint(  
  value: number | bigint,  
  bits: number = 64,  
) : bigint { }
```

Transforms a signed integer (JS Number) `value` into an unsigned integer of `bits` number of bits.

E.g.:

```
CAPI.FP.int2uint(-5);
```

CAPI.FP.uint2int

```
CAPI.FP.uint2int(value: number | bigint): bigint { }
```

Transforms an unsigned integer `value` into a signed integer (JS Number) of `bits` number of bits.

E.g.:

```
CAPI.FP.uint2int(5);
```

CAPI.FP.uint2float64

```
CAPI.FP.uint2float64(value0: number | bigint, value1?: number): number { }
```

Transforms an unsigned integer `value0` into a signed integer to a 64-bit float (JS Number). Supports two calling conventions: 1. Single `value0` argument: converts a 64-bit integer directly 2. Two 32-bit arguments: converts low (`value0`) and high (`value1`) 32-bit parts.

E.g.:

```
CAPI.FP.uint2float64(5);
```

CAPI.FP.float642uint

```
CAPI.FP.float642uint(value: number): [number, number] { }
```

Transforms the double precision floating point (JS Number) `value` into an unsigned integer.

E.g.:

```
CAPI.FP.float642uint(5.0);
```

CAPI.FP.check_ieee

```
CAPI.FP.check_ieee(sign: string, exponent: string, mantissa: string): number { }
```

Check the type of number is in IEEE 754 format. Returns a 10-bit mask where the position of the set bit indicates the type of the IEEE 754 number:

- - 0 -> -inf
- - 1 -> -normalized number
- - 2 -> -non-normalized number
- - 3 -> -0
- - 4 -> +0
- - 5 -> +non-normalized number
- - 6 -> +normalized number
- - 7 -> +inf
- - 8 -> signaling NaN
- - 9 -> quiet NaN

E.g.:

```
CAPI.FP.check_ise(parseInt(a[0]), parseInt(a.slice(1,9), 2), parseInt(a.slice(10), 2));
```

CAPI.FP.float2bin

```
CAPI.FP.float2bin(f: number): string { }
```

Transforms the single precision floating point JS Number `f` into a binary string.

E.g.:

```
CAPI.FP.float2bin(5.0);
```

Registers

CAPI.REG.read

```
CAPI.REG.read(name: string): bigint { }
```

Returns the value stored in register `name`.

E.g.:

```
const foo = CAPI.REG.read("t0");
```

CAPI.REG.write

```
CAPI.REG.write(value: bigint, name: string): void { }
```

Stores `value` in register `name`.

E.g.:

```
CAPI.REG.write(0x69n, "t0");
```

Architecture

`CAPI.ARCH` exposes the interface of the currently loaded architecture plugin.

The supported plugins are `riscv`, `mips` and `z80`.

RISC-V

The RISC-V architecture plugin provides utilities for handling floating point operations and immediate value generation.

generateLoadImmediate

```
CAPI.ARCH.generateLoadImmediate(val: bigint | number, destReg: string): string { }
```

Generates a sequence of RISC-V instructions to load an immediate value into a register. Returns a semicolon-separated string of instructions that can load values of any size into the destination register.

E.g.:

```
const instructions = CAPI.ARCH.generateLoadImmediate(0x12345678n, "t0");
// Returns: "lui t0, 0x12345;addiw t0, t0, 1656"
```

toJSNumberD

```
CAPI.ARCH.toJSNumberD(bigIntValue: bigint): [number, string] { }
```

Converts a 64-bit register value to a JavaScript number when the D (double-precision floating point) extension is enabled. Returns a tuple containing the numeric value and a type string indicating the representation.

The function handles:

- - Canonical 64-bit NaN (0x7ff800000000000n) → [NaN, "NaN64"]
- - NaN-boxed 32-bit floats (upper 32 bits all 1's) → [value, "NaNBfloat32_64"]
- - Valid 64-bit doubles → [value, "float64"] - Zero → [0, "float32"]

E.g.:

```
let value, type;
[value, type] = CAPI.ARCH.toJSNumberD(registers.ft0);
```

toJSNumberS

```
CAPI.ARCH.toJSNumberS(bigIntValue: bigint): [number, string] { }
```

Converts a 32-bit register value to a JavaScript number when only the S (single-precision floating point) extension is enabled. Returns a tuple containing the numeric value and a type string.

The function handles: - Canonical 32-bit NaN (0x7fc00000n) → [NaN, "NaN32"] - Valid 32-bit floats → [value, "float32"] - Zero → [0, "float32"]

E.g.:

```
let value, type;
[value, type] = CAPI.ARCH.toJSNumberS(registers.ft0);
```

toBigInt

```
CAPI.ARCH.toBigInt(number: number, type: string): bigint { }
```

Converts a JavaScript number to a bigint representation suitable for storing in a RISC-V register. The `type` parameter specifies the format.

Supported types:

- - "float32": Single-precision float
- - "float64": Double-precision float
- - "NaNbfloat32_64": NaN-boxed single-precision (upper 32 bits all 1's)
- - "NaN64": Canonical 64-bit NaN
- - "NaN32": Canonical 32-bit NaN

E.g.:

```
registers.ft0 = CAPI.ARCH.toBigInt(3.14, "float32");
```

NaNBox

```
CAPI.ARCH.NaNBox(bigIntValue: bigint): bigint { }
```

NaN-boxes a 32-bit floating point value for use in 64-bit floating point registers. Sets the upper 32 bits to all 1's as per the RISC-V specification (section 21.2).

E.g.:

```
const nanBoxed = CAPI.ARCH.NaNBox(registers.ft0);
```

MIPS

The MIPS architecture plugin provides utilities for handling double-precision floating point operations across register pairs.

validateEvenRegister

```
CAPI.ARCH.validateEvenRegister(regName: string): void { }
```

Validates that a register number is even. Required for double-precision operations in MIPS, which use register pairs. Throws an error if the register is not even.

E.g.:

```
CAPI.ARCH.validateEvenRegister("f0"); // OK
CAPI.ARCH.validateEvenRegister("f1"); // Throws error
```

readDouble

```
CAPI.ARCH.readDouble(regName: string): number { }
```

Reads a double-precision floating point value from a MIPS register pair. The `regName` must be even (e.g., "f0", "f2"). The function reads from the specified register and the next sequential register to reconstruct a 64-bit double.

E.g.:

```
const value = CAPI.ARCH.readDouble("f0"); // Reads f0 and f1
```

writeDouble

```
CAPI.ARCH.writeDouble(value: number, regName: string): void { }
```

Writes a double-precision floating point value to a MIPS register pair. The `regName` must be even. The function splits the value across the specified register and the next sequential register.

E.g.:

```
CAPI.ARCH.writeDouble(3.14159, "f0"); // Writes to f0 and f1
```

readDoublePair

```
CAPI.ARCH.readDoublePair(reg1Name: string, reg2Name: string): number[] { }
```

Reads two double-precision values from register pairs and returns them as an array. Both register names must be even.

E.g.:

```
const [val1, val2] = CAPI.ARCH.readDoublePair("f0", "f2");
```

writeDoublePair

```
CAPI.ARCH.writeDoublePair(value1: number, value2: number, reg1Name: string, reg2Name: string): void { }
```

Writes two double-precision values to register pairs. Both register names must be even.

E.g.:

```
CAPI.ARCH.writeDoublePair(1.5, 2.5, "f0", "f2");
```

binaryDoubleOperation

```

CAPI.ARCH.binaryDoubleOperation(
    destReg: string,
    src1Reg: string,
    src2Reg: string,
    operation: (val1: number, val2: number) => number
): void { }

```

Performs a binary operation on two double-precision values. Reads from source register pairs, applies the operation function, and writes the result to the destination register pair. All register names must be even.

E.g.:

```
CAPI.ARCH.binaryDoubleOperation("f0", "f2", "f4", (a, b) => a + b);
```

unaryDoubleOperation

```

CAPI.ARCH.unaryDoubleOperation(
    destReg: string,
    srcReg: string,
    operation: (val: number) => number
): void { }

```

Performs a unary operation on a double-precision value. Reads from the source register pair, applies the operation function, and writes the result to the destination register pair. Both register names must be even.

E.g.:

```
CAPI.ARCH.unaryDoubleOperation("f0", "f2", (x) => Math.sqrt(x));
```

Z80

The Z80 architecture plugin provides utilities for flag calculations, keyboard handling, and I/O operations.

Flag Constants The following flag bit masks are available:

```

CAPI.ARCH.S_FLAG // 0x80 - Sign flag
CAPI.ARCH.Z_FLAG // 0x40 - Zero flag
CAPI.ARCH.H_FLAG // 0x10 - Half-carry flag

```

```
CAPI.ARCH.PV_FLAG // 0x04 - Parity/Overflow flag
CAPI.ARCH.N_FLAG  // 0x02 - Add/Subtract flag
CAPI.ARCH.C_FLAG  // 0x01 - Carry flag
```

State Variables The following variables track the Z80 system state:

```
CAPI.ARCH.borderColor // Border color (0-7) for ZX Spectrum
CAPI.ARCH.interruptMode // Current interrupt mode (0, 1, or 2)
CAPI.ARCH.interruptPin // Interrupt pin state (0 = low, 1 = high)
CAPI.ARCH.timerCounter // Timer counter value (bigint)
CAPI.ARCH.keyState // Object mapping event.code strings to pressed state (boolean)
CAPI.ARCH.keyMap // Keyboard matrix mapping port high bytes to key codes
```

E.g.:

```
// Set interrupt mode 2
CAPI.ARCH.interruptMode = 2;

// Check if a key is pressed
if (CAPI.ARCH.keyState["KeyA"]) {
  // Key A is pressed
}

// Set border color to red
CAPI.ARCH.borderColor = 2n;
```

calculateFlags_INC

```
CAPI.ARCH.calculateFlags_INC(oldValue: bigint, initialF: bigint): bigint { }
```

Calculates flags for an 8-bit INC (increment) operation. Returns the new F register value with appropriate flags set. The C flag is preserved from initialF.

E.g.:

```
registers.F = CAPI.ARCH.calculateFlags_INC(registers.A, registers.F);
```

calculateFlags_DEC

```
CAPI.ARCH.calculateFlags_DEC(oldValue: bigint, initialF: bigint): bigint { }
```

Calculates flags for an 8-bit DEC (decrement) operation. Returns the new F register value. The C flag is preserved, and N flag is always set.

E.g.:

```
registers.F = CAPI.ARCH.calculateFlags_DEC(registers.A, registers.F);
```

calculateFlags_ADD

```
CAPI.ARCH.calculateFlags_ADD(val1: bigint, val2: bigint): bigint { }
```

Calculates flags for 8-bit addition (ADD). Returns the new F register value with all flags computed based on the operation.

E.g.:

```
registers.F = CAPI.ARCH.calculateFlags_ADD(registers.A, registers.B);
```

calculateFlags_ADC

```
CAPI.ARCH.calculateFlags_ADC(val1: bigint, val2: bigint, initialF: bigint): bigint { }
```

Calculates flags for 8-bit addition with carry (ADC). The carry bit is extracted from initialF.

E.g.:

```
registers.F = CAPI.ARCH.calculateFlags_ADC(registers.A, registers.B, registers.F);
```

calculateFlags_SUB

```
CAPI.ARCH.calculateFlags_SUB(val1: bigint, val2: bigint): bigint { }
```

Calculates flags for 8-bit subtraction (SUB). The N flag is always set for subtraction operations.

E.g.:

```
registers.F = CAPI.ARCH.calculateFlags_SUB(registers.A, registers.B);
```

calculateFlags_SBC

```
CAPI.ARCH.calculateFlags_SBC(val1: bigint, val2: bigint, initialF: bigint): bigint { }
```

Calculates flags for 8-bit subtraction with carry (SBC). The carry bit is extracted from initialF.

E.g.:

```
registers.F = CAPI.ARCH.calculateFlags_SBC(registers.A, registers.B, registers.F);
```

calculateFlags_LOGICAL

```
CAPI.ARCH.calculateFlags_LOGICAL(result: bigint, setH: number): bigint { }
```

Calculates flags for logical operations (AND, OR, XOR). Set `setH` to 1 for AND operations (sets H flag), or 0 for OR/XOR operations (resets H flag). N and C flags are always reset.

E.g.:

```
registers.F = CAPI.ARCH.calculateFlags_LOGICAL(registers.A & registers.B, 1);
```

calculateFlags_CP

```
CAPI.ARCH.calculateFlags_CP(val1: bigint, val2: bigint): bigint { }
```

Calculates flags for the compare (CP) operation. Performs a subtraction for flag calculation purposes without storing the result.

E.g.:

```
registers.F = CAPI.ARCH.calculateFlags_CP(registers.A, registers.B);
```

calculateFlags_ADD16

```
CAPI.ARCH.calculateFlags_ADD16(val1: bigint, val2: bigint, initialF: bigint): bigint { }
```

Calculates flags for 16-bit addition (ADD HL, rr). The S, Z, and P/V flags are preserved from `initialF`. N flag is reset.

E.g.:

```
registers.F = CAPI.ARCH.calculateFlags_ADD16(registers.HL, registers.BC, registers.F);
```

calculateFlags_SBC16

```
CAPI.ARCH.calculateFlags_SBC16(val1: bigint, val2: bigint, initialF: bigint): bigint { }
```

Calculates flags for 16-bit subtraction with carry (SBC HL, rr). The carry bit is extracted from `initialF`.

E.g.:

```
registers.F = CAPI.ARCH.calculateFlags_SBC16(registers.HL, registers.BC, registers.F);
```

calculateFlags_BIT

```
CAPI.ARCH.calculateFlags_BIT(value: bigint, bit: number, initialF: bigint): bigint { }
```

Calculates flags for the BIT instruction, which tests a specific bit (0-7) in a value. The C flag is preserved from `initialF`, and H flag is always set. N flag is always reset.

E.g.:

```
registers.F = CAPI.ARCH.calculateFlags_BIT(registers.A, 7, registers.F);
```

calculateFlags_ROTATE

```
CAPI.ARCH.calculateFlags_ROTATE(result: bigint, carry: bigint): bigint { }
```

Calculates flags for rotate and shift instructions (RLC, RRC, SLA, etc.). The `carry` parameter should be `0n` or `1n` representing the bit that was shifted out. H and N flags are always reset.

E.g.:

```
const carry = registers.A >> 7n;
const result = ((registers.A << 1n) | carry) & 0xffn;
registers.F = CAPI.ARCH.calculateFlags_ROTATE(result, carry);
```

calculateFlags_SRL

```
CAPI.ARCH.calculateFlags_SRL(result: bigint, carry: bigint): bigint { }
```

Calculates flags for the SRL (Shift Right Logical) instruction. The `carry` parameter is the original bit 0 that was shifted out. S, H, and N flags are always reset.

E.g.:

```
const carry = registers.A & 1n;
const result = registers.A >> 1n;
registers.F = CAPI.ARCH.calculateFlags_SRL(result, carry);
```

pressKey

```
CAPI.ARCH.pressKey(code: string): void { }
```

Registers a keyboard key as being pressed. The `code` parameter should be a JavaScript `event.code` string (e.g., "KeyA", "Digit1").

E.g.:

```
CAPI.ARCH.pressKey("KeyA");
```

releaseKey

```
CAPI.ARCH.releaseKey(code: string): void { }
```

Registers a keyboard key as being released.

E.g.:

```
CAPI.ARCH.releaseKey("KeyA");
```

readULAKeyboard

```
CAPI.ARCH.readULAKeyboard(port: bigint): bigint { }
```

Emulates a read from the ZX Spectrum ULA keyboard port. The high byte of the port address determines which half-row of keys to poll. Returns an 8-bit value where bits 0-4 represent key states (0 = pressed, 1 = not pressed), and bits 5-7 are typically high.

E.g.:

```
const keyState = CAPI.ARCH.readULAKeyboard(0xf7fen); // Read row with keys 1-5
```

read

```
CAPI.ARCH.read(port: bigint): bigint { }
```

Reads a byte from an I/O port. Handles: - Port 0x01: Keyboard buffer (non-blocking) - ULA ports (keyboard matrix): ZX Spectrum keyboard - Unhandled ports: Returns 0xFF

E.g.:

```
const value = CAPI.ARCH.read(0x01n); // Read from keyboard buffer
```

write

```
CAPI.ARCH.write(port: bigint, value: bigint): void { }
```

Writes a byte to an I/O port. Handles:

- - Port 0x02: Screen output
- - Port 0xFE: ZX Spectrum ULA (sets border color from bits 0-2)
- - Port 0x17: CREATOR-specific port for ecall (exits on value 10n)

E.g.:

```
CAPI.ARCH.write(0x02n, 65n); // Write 'A' to screen
CAPI.ARCH.write(0xfen, 0x02n); // Set border color to red
```

Interrupts

Functions to manage interrupts and privilege modes.

For more information, see Interrupt Support.

CAPI.INTERRUPTS.setUserMode

```
CAPI.INTERRUPTS.setUserMode(): void { }
```

Sets the privilege level to User.

E.g.:

```
CAPI.INTERRUPTS.setUserMode();
```

CAPI.INTERRUPTS.setKernelMode

```
CAPI.INTERRUPTS.setKernelMode(): void { }
```

Sets the privilege level to Kernel.

E.g.:

```
CAPI.INTERRUPTS.setKernelMode();
```

CAPI.INTERRUPTS.create

```
CAPI.INTERRUPTS.create(type: InterruptType): void { }
```

Creates an interrupt of the specified type.

E.g.:

```
CAPI.INTERRUPTS.create(InterruptType.Software);
```

CAPI.INTERRUPTS.enable

```
CAPI.INTERRUPTS.enable(type: InterruptType): void { }
```

Enables an interrupt type.

E.g.:

```
CAPI.INTERRUPTS.enable(InterruptType.Software);
```

CAPI.INTERRUPTS.globalEnable

```
CAPI.INTERRUPTS.globalEnable(): void { }
```

Globally enables interrupts.

E.g.:

```
CAPI.INTERRUPTS.globalEnable();
```

CAPI.INTERRUPTS.disable

```
CAPI.INTERRUPTS.disable(type: InterruptType): void { }
```

Disables an interrupt type.

E.g.:

```
CAPI.INTERRUPTS.disable(InterruptType.Software);
```

CAPI.INTERRUPTS.globalDisable

```
CAPI.INTERRUPTS.globalDisable(): void { }
```

Globally disables interrupts.

E.g.:

```
CAPI.INTERRUPTS.globalDisable();
```

CAPI.INTERRUPTS.isEnabled

```
CAPI.INTERRUPTS.isEnabled(type: InterruptType): boolean { }
```

Checks if an interrupt type is enabled.

E.g.:

```
CAPI.INTERRUPTS.isEnabled(InterruptType.Software);
```

CAPI.INTERRUPTS.isGlobalEnabled

```
CAPI.INTERRUPTS.isGlobalEnabled(): boolean { }
```

Checks if interrupts are globally enabled.

E.g.:

```
CAPI.INTERRUPTS.isGlobalEnabled();
```

CAPI.INTERRUPTS**.clear**

```
CAPI.INTERRUPTS.clear(type: InterruptType): void { }
```

Clears interrupts of the specified type.

E.g.:

```
CAPI.INTERRUPTS.clear(InterruptType.Software);
```

CAPI.INTERRUPTS**.globalClear**

```
CAPI.INTERRUPTS.globalClear(): void { }
```

Clears all interrupts.

E.g.:

```
CAPI.INTERRUPTS.globalClear();
```

CAPI.INTERRUPTS**.setCustomHandler**

```
CAPI.INTERRUPTS.setCustomHandler(): void { }
```

Sets the interrupt handler to the custom handler.

E.g.:

```
CAPI.INTERRUPTS.setCustomHandler();
```

CAPI.INTERRUPTS**.setCREATORHandler**

```
CAPI.INTERRUPTS.setCREATORHandler(): void { }
```

Sets the interrupt handler to the default CREATOR handler.

E.g.:

```
CAPI.INTERRUPTS.setCREATORHandler();
```

CAPI.INTERRUPTS.setHighlight

```
CAPI.INTERRUPTS.setHighlight(): void { }
```

Highlights the current instruction as “interrupted” in the UI.

E.g.:

```
CAPI.INTERRUPTS.setHighlight();
```

CAPI.INTERRUPTS.clearHighlight

```
CAPI.INTERRUPTS.setHighlight(): void { }
```

Removes the “interrupted” highlight in the UI. Typically used in instructions that return from the interrupt handler, such as RISC-V’s `mret`.

E.g.:

```
CAPI.INTERRUPTS.clearHighlight();
```

Creating Custom Architectures

CREATOR supports defining custom architectures through YAML configuration files. This allows adding new instruction sets or modifying existing ones.

Creating an Architecture File

An architecture file is a YAML file that describes the architecture’s properties, including its instruction set, registers, memory layout, and other relevant details. Instructions are defined with their binary encoding, assembly syntax, and semantics.



We provide a JSON schema for the architecture file at <https://creatorsim.github.io/creator/schema/architecture.json>.

The actual definition for an instruction is a simple JavaScript code block to manipulate the simulator state. Within this block, you have the `registers` variable to access the registers (e.g. `registers.PC`, or `registers[value]`), as well as `CAPI`, an API that allows you to interact with the simulator.



The values stored in the registers are `BigInt`. Take that into account when reading or writing values:

```
1 const foo = registers.PC; // 420n
2 registers.PC = foo + 1n; // 421n
```

Let's define a simple 8-bit architecture with a few instructions.

The first step is to create a YAML file, e.g., `simplearch.yml`, and fill out the `config`. We want an architecture where the word size and byte size are both 8 bits. We'll also make it little-endian, although it doesn't matter in this specific case because a word contains only one byte. `pc_offset` will be 0. The entry point will be a function named `main`, or address `0x0` if it doesn't exist; we'll use the `;` character to write comments, and the names of the registers won't be sensitive (`PC == pc`). We'll also enable memory alignment and passing convention checks.



The value of the program counter register (`program_counter`) inside the instruction definitions is affected by the `pc_offset`.

`pc_offset` is the offset that we'll add to the value of program counter the instruction "sees".

E.g. if `pc_offset` is `-4`, and we're executing an instruction at `0x0`, the "real" PC is `0x4` (because of the fetch performed at the start of the cycle), but the value of `registers.PC` (the "virtual" PC) will be `0x0`.

```
version: 2.0.0
config:
  name: Simple8Bit
  description: A simple custom 8-bit architecture
  word_size: 8
  byte_size: 8
  endianness: little_endian
  pc_offset: 0
  main_function: main
  start_address: 0x0
  comment_prefix: ;
  sensitive_register_name: false
  memory_alignment: true
  passing_convention: true
```

For the registers, we'll make a control register bank with a PC program counter register (we'll mark that with the `program_counter` property), and another integer register bank with a A and B register, as well as a SP stack pointer register (`stack_pointer` property).



A floating point bank would be defined as:

```

1 # ...
2 - name: Floating point registers
3   type: fp_registers
4   double_precision: true # or 'false', if single-precision

```

All of these registers will be 8 bits, be initialized (`value`) and have a default value (`default_value`) of 0, and will be both readable (`read` property) and writable (`write` property).



The `encoding` property will be used when decoding binary instructions, in this case we'll just make it sequential.

`name` is a list because a register can have multiple values, e.g. in RISC-V register `zero` can be also called `x0`, and so on. These names must all be unique.

components:

```

- name: Control registers
  type: ctrl_registers
  double_precision: false
  elements:
    - name:
      - PC
      nbits: 8
      encoding: 0
      value: 0
      default_value: 0
      properties:
        - read
        - write
        - program_counter
- name: Integer registers
  type: int_registers
  double_precision: false
  elements:
    - name:
      - A
      encoding: 0
      nbits: 8
      value: 0
      default_value: 0
      properties:
        - read

```

```

    - write
- name:
  - B
  encoding: 1
  nbits: 8
  value: 0
  default_value: 0
  properties:
    - read
    - write
- name:
  - SP
  encoding: 2
  nbits: 8
  value: 0
  default_value: 0
  properties:
    - read
    - write
    - stack_pointer

```

For the memory layout, we'll use a simple `.text`, `.data`, `.stack` layout:

```

memory_layout:
  text:
    start: 0x0000
    end: 0x03FF
  data:
    start: 0x0400
    end: 0x7FFF
  stack:
    start: 0x8000
    end: 0xFFFF

```

Now it's time for the instructions. We want an architecture with two instructions: `NOP` and `ADD` in the `base` extension. The `NOP` instruction does nothing, while the `ADD` instruction adds the values of two registers and stores the result in a destination register.

As the instructions will have the same form, we can define an instruction template called `standard` defining that our instructions will be 1 word long (`nwords`), take 1 clock cycle (`clk_cycles`) and use the full word as an operation code (type `co`) field. We then override in each instruction the value of that field.

```

templates:

```

```
- name: standard
  nwords: 1
  clk_cycles: 1
  fields:
    - name: opcode
      type: co
      startbit: 7
      stopbit: 0
      order: 0

instructions:
  base:
    - name: nop
      template: standard
      fields:
        - field: opcode
          value: "0x00"
      definition: ""

    - name: add
      template: standard
      fields:
        - field: opcode
          value: "0x80"
      definition: |
        const oldValueA = registers.A;
        registers.A = (oldValueA + registers.B) & 0xFFn;
        registers.F = CAPI.ARCH.calculateFlags_ADD(oldValueA, registers.B);

directives:
  - name: .data
    action: data_segment
    size: null
  - name: .text
    action: code_segment
    size: null
  - name: .bss
    action: global_symbol
    size: null
  - name: .zero
    action: space
    size: 1
```

```
- name: .space
  action: space
  size: 1
- name: .align
  action: align
  size: null
- name: .balign
  action: balign
  size: null
- name: .globl
  action: global_symbol
  size: null
- name: .string
  action: ascii_null_end
  size: null
- name: .asciz
  action: ascii_null_end
  size: null
- name: .ascii
  action: ascii_not_null_end
  size: null
- name: .byte
  action: byte
  size: 1
- name: .half
  action: half_word
  size: 2
- name: .word
  action: word
  size: 4
- name: .dword
  action: double_word
  size: 8
- name: .float
  action: float
  size: 4
- name: .double
  action: double
  size: 8
```

Plugins

Interrupt Support

Now, let's take our architecture and add support for some simple maskable and nonmaskable interrupts.

Custom handler

We'll define two new 1-bit integer registers MIP (*Maskable Interrupt Pending*) and NIP (*Nonmaskable Interrupt Pending*) that will be set to 1 when an interrupt of the type is pending. We'll also define another 1-bit integer register IE to enable (value of 1) and disable (value of 0) maskable interrupts.

We just need to add them to `simplearch.yml`:

```
components:
  # ...
  - name: Integer registers
    # ...
    elements:
      # ...
      - name:
          - MIP
        encoding: 2
        nbits: 1
        value: 0
        default_value: 0
        properties:
          - read
          - write
      - name:
          - NIP
        encoding: 3
        nbits: 1
        value: 0
        default_value: 0
        properties:
          - read
          - write
      - name:
          - IE
        encoding: 4
        nbits: 1
        value: 1
```

```

default_value: 1
properties:
  - read
  - write

```

Now we have to define some functions to determine how interrupts work in this architecture.

First, we need to define how to determine if an interrupt happened. CREATOR has some predefined types of interrupts, and here we'll use `InterruptType.Maskable` and `InterruptType.Nonmaskable`. We have to write a function that returns the type of interrupt (`InterruptType`), or null if there is no interrupt:



You don't have to check if interrupts are enabled here, we'll define that later.

```

interrupts:
  check: |
    if (registers.NIP) return InterruptType.Nonmaskable;
    if (registers.MIP) return InterruptType.Maskable;
    return null;

```

Then, we must define how different types of interrupts can be created and cleared. We'll receive the desired type (`InterruptType`) inside the `type` variable:

```

interrupts:
  # ...
  create: |
    switch (type) {
      case InterruptType.Maskable:
        registers.MIP = 1n;
        break;
      case InterruptType.Nonmaskable:
        registers.NIP = 1n;
        break;
    }

  clear: |
    switch (type) {
      case InterruptType.Maskable:
        registers.MIP = 0n;
        break;
      case InterruptType.Nonmaskable:
        registers.NIP = 0n;

```

```

        break;
    }

global_clear: |
    registers.MIP = 0n;
    registers.NIP = 0n;

```



clear is optional, it gets overridden by `global_clear` if it's not defined

Next, how they can be enabled and disabled, per type (and globally), as well as how to check if they are enabled. For the sake of simplicity, we'll assume nonmaskable interrupts can't be disabled.

```

# ...
interrupts:
# ...
is_enabled: |
    switch (type) {
        case InterruptType.Maskable:
            return registers.MIE === 1n;
        case InterruptType.Nonmaskable:
            // nonmaskable are always enabled
            return true;
    }
    return false;

is_global_enabled: |
    return true;

enable: |
    switch (type) {
        case InterruptType.Maskable:
            return registers.MIE = 1n;
            break;
        // we don't need to do anything for nonmaskable
    }

disable: |
    switch (type) {
        case InterruptType.Maskable:
            registers.IE = 0n;
            break;
    }

```

```

    // can't disable nonmaskable
}

global_enable: |
    registers.IE = 1n;

global_disable: |
    registers.IE = 0n;

```



enable and disable are optional, they gets overridden by global_ counterparts if it's not defined. is_global_enabled is optional, and defaults to return true.

Finally, we define the custom interrupt handler. This handler will disable interrupts, store PC in the stack, and jump to 0x0. To disable interrupts, we do it “manually” by clearing IE, but we can also use CAPI to reuse the code we already defined.



Using these CAPI functions is recommended way of doing it, as it allows the application to (secretly) keep track of these interrupts.

```

interrupts:
  handlers:
    custom: |
      // disable interrupt
      CAPI.INTERRUPTS.disable(type);

      // store PC in stack
      registers.SP = (registers.SP - 1n) & 0xFFn;
      CAPI.MEM.write(registers.SP, 1, registers.PC);

      // jump to handler
      registers.PC = 0n;

```

Many architectures have a specific instruction to return from an interrupt, so let's make one, `reti`. This instruction will clear and enable interrupts and jump back to the address stored in the stack:

```

instructions:
  base:
    # ...
    - name: reti
      template: standard
      fields:

```

```

- field: opcode
  value: "0x01"
definition: |
  // enable interrupts
  CAPI.INTERRUPTS.globalEnable();

  // pop return address from stack
  registers.PC = CAPI.MEM.read(registers.SP, 1);
  registers.SP = (registers.SP + 1n) & 0xFFn;

  // notify UI that handler has finished
  CAPI.INTERRUPTS.clearHighlight();

```

CREATOR handler

As we mentioned in Interrupt Handling, CREATOR has two different interrupt handlers: the default “CREATOR” one, and a custom architecture-defined one. We also mentioned that the default handler is able to handle “architecture-defined system calls”. Let’s see a more concrete example, by implementing them in our architecture.



Why would we want this? Because we want to have our cake and eat it too. Before interrupts were added to CREATOR, the definition of RISC-V’s `ecall` function didn’t create an interrupt, it just executed the desired system call depending on the value of register `a7`. But we wanted to have “real” interrupts and a “real” `ecall`. The problem is that this required an interrupt handler, and we didn’t want to force our users to use it, we didn’t want to silently include a kernel, and we didn’t want to have two architectures: one with interrupts and one without. So the solution (compromise) we found was this one, a second (default) interrupt handler that can be programmed in JS.

These system calls will generate a new type of interrupt (`InterruptType.EnvironmentCall`), so let’s quickly modify the architecture to take them into account. We’ll also add a new EIP register to signal that that type of interrupt is pending.

```

components:
  # ...
  - name: Integer registers
    # ...
  elements:
    # ...
    - name:
      - EIP

```

```
    encoding: 2
    nbits: 1
    value: 0
    default_value: 0
    properties:
      - read
      - write

# ...

interrupts:
  check: |
    if (registers.NIP) return InterruptType.Nonmaskable;
    if (registers.MIP) return InterruptType.Maskable;
    if (registers.EIP) return InterruptType.EnvironmentCall;
    return null;

  is_enabled: |
    switch (type) {
      case InterruptType.Maskable:
        return registers.MIE === 1n;
      case InterruptType.EnvironmentCall:
        return registers.EIE === 1n;
      case InterruptType.Nonmaskable:
        // nonmaskable are always enabled
        return true;
    }
    return false;

  enable: |
    switch (type) {
      case InterruptType.Maskable:
        // we don't need to do anything for nonmaskable
        break;
      default:
        registers.IE = 1n;
        break;
    }

  disable: |
    switch (type) {
      case InterruptType.Maskable:
        // can't disable nonmaskable
```

```

        break;
    default:
        registers.IE = 0n;
        break;
    }

create: |
    switch (type) {
        case InterruptType.Maskable:
            registers.MIP = 1n;
            break;
        case InterruptType.Nonmaskable:
            registers.NIP = 1n;
            break;
        case InterruptType.EnvironmentCall:
            registers.EIP = 1n;
            break;
    }

clear: |
    switch (type) {
        case InterruptType.Maskable:
            registers.MIP = 0n;
            break;
        case InterruptType.Nonmaskable:
            registers.NIP = 0n;
            break;
    }

global_clear: |
    registers.MIP = 0n;
    registers.NIP = 0n;
    registers.EIP = 0n;

# ...

```

Now we can define our `syscall` instruction:

```

# ...
instructions:
    base:
        # ...

```

```

- name: syscall
  template: standard
  fields:
    - field: opcode
      value: "0x02"
  definition: CAPI.INTERRUPTS.create(InterruptType.EnvironmentCall);

```

The convention will be that the type of system call we want to use will be stored in register A, while register B will hold extra information. For example, a system call to print a number will print whatever B is holding.

To allow CREATOR's handler to handle them, as system calls depend on each architecture, we must define that in the architecture definition:

```

# ...
interrupts:
  handlers:
    # ...
    creator_syscall: |
      switch (registers.A) {
        case 1n:
          CAPI.SYSCALL.print(registers.B, 'int32');
          break;
      }

      // notify UI that handler has finished
      CAPI.INTERRUPTS.clearHighlight();

```

Privileged instructions

CREATOR also supports having privileged instructions that can only be executed in kernel mode, by adding the `privileged` property. This is the reason for having system calls in the first place, we allow the user to ask doing things that require a higher privilege (e.g. accessing I/O) without giving them that privilege itself.

Let's say that in our architecture, an interrupt always triggers an execution mode change. To achieve that, we should modify the custom handler so that it sets kernel mode (`CAPI.INTERRUPTS.setKernelMode();`) and modify the `reti` instruction so that it goes back to user mode (`CAPI.INTERRUPTS.setUserMode();`). As `reti` should only be used while dealing with interrupts, we'll make it a privileged instruction.

```

instructions:
  base:

```

```
# ...
- name: reti
  # ...
  properties:
    - privileged
  definition: |
    // enable interrupts
    CAPI.INTERRUPTS.globalEnable();

    // pop return address from stack
    registers.PC = CAPI.MEM.read(registers.SP, 1);
    registers.SP = (registers.SP + 1n) & 0xFFn;

    // notify UI that handler has finished
    CAPI.INTERRUPTS.clearHighlight();

    // set user mode
    CAPI.INTERRUPTS.setUserMode();

# ...

interrupts:
  handlers:
    custom: |
      // disable interrupt
      CAPI.INTERRUPTS.disable(type);

      // set kernel mode
      CAPI.INTERRUPTS.setKernelMode();

      // store PC in stack
      registers.SP = (registers.SP - 1n) & 0xFFn;
      CAPI.MEM.write(registers.SP, 1, registers.PC);

      // jump to handler
      registers.PC = 0n;
```

Validating program execution

The CREATOR CLI allows to validate the execution of a program.

For this, you first need to define a YAML validator file. This file must contain the expected final

state of the program, as well as any additional options you want to set for the validation.

Validator File



We provide a JSON schema for the validator file at <https://creator-sim.github.io/creator/schema/validator-file.json>.

The validator file is a YAML file that can contain the following fields: - **maxCycles**: The maximum number of cycles to run the program for validation. If the program exceeds this number of cycles, it will be considered invalid. - **floatThreshold**: The maximum allowed error for floating point register comparisons. - **sentinel**: A boolean indicating whether to enable sentinel checking (calling convention errors). - **state**: An object defining the expected final state of the program, which can contain: - **registers**: A mapping of integer register names to their expected values. - **floatRegisters**: A mapping of floating point register names to their expected values. - **memory**: A mapping of memory addresses (as strings) to their expected byte values. - **display**: The expected contents of the display buffer as a string.

The validator will return, following POSIX conventions, 0 if its valid and 1 if it's not, writing the error message to the standard error stream (stderr).

Example

Quick example of a validator file:

```
maxCycles: 100
floatThreshold: 10e-10
sentinel: true
state:
  floatRegisters:
    f0: 0x40866666
  registers:
    sp: 0xFFFFFC
    a1: 0x000005A
  memory:
    "0x200000": 0x45
  display: "-144"
```

Using the Validator

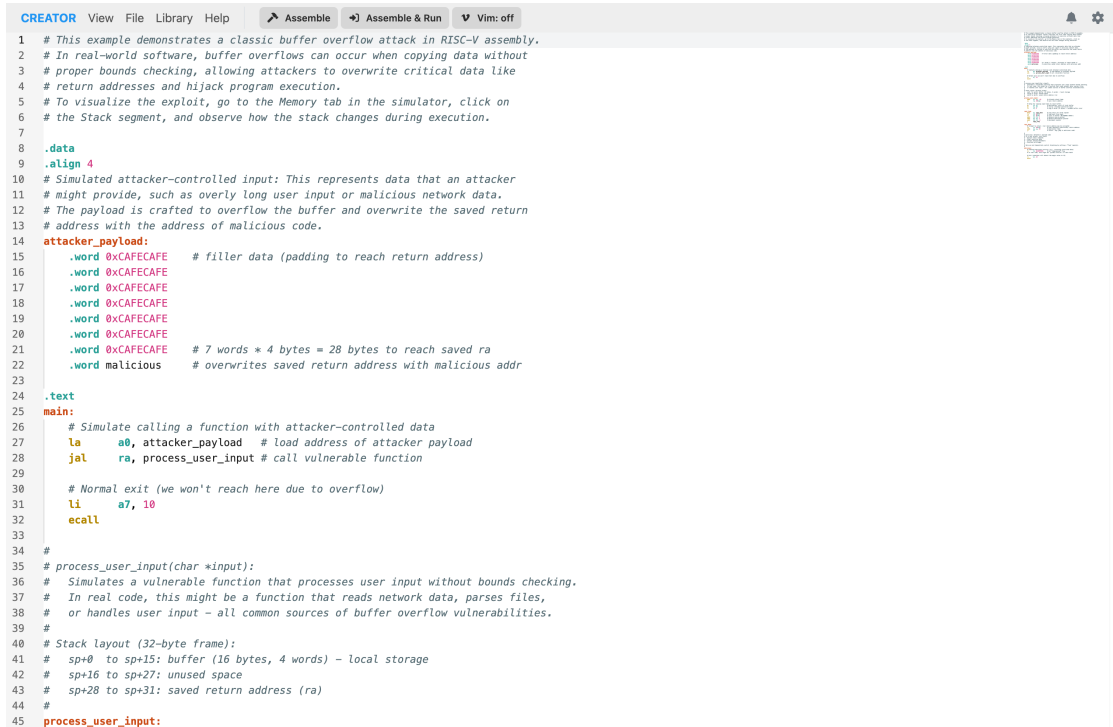
To use the validator file with CREATOR CLI, use the `--validate` option followed by the path to the validator YAML file.

For example:

```
1 creator-cli -a RV32IMFD.yml -s assembly.s --validate config.yml
```

Web Version Overview

CREATOR is a browser-based assembly programming environment that requires no installation. It provides a complete development and debugging environment for multiple architectures directly in your web browser.



```

CREATOR View File Library Help Assemble Assemble & Run Vim: off
1 # This example demonstrates a classic buffer overflow attack in RISC-V assembly.
2 # In real-world software, buffer overflows can occur when copying data without
3 # proper bounds checking, allowing attackers to overwrite critical data like
4 # return addresses and hijack program execution.
5 # To visualize the exploit, go to the Memory tab in the simulator, click on
6 # the Stack segment, and observe how the stack changes during execution.
7
8 .data
9 .align 4
10 # Simulated attacker-controlled input: This represents data that an attacker
11 # might provide, such as overly long user input or malicious network data.
12 # The payload is crafted to overflow the buffer and overwrite the saved return
13 # address with the address of malicious code.
14 attacker_payload:
15     .word 0xCAFECAFE # filler data (padding to reach return address)
16     .word 0xCAFECAFE
17     .word 0xCAFECAFE
18     .word 0xCAFECAFE
19     .word 0xCAFECAFE
20     .word 0xCAFECAFE
21     .word 0xCAFECAFE # 7 words * 4 bytes = 28 bytes to reach saved ra
22     .word malicious # overwrites saved return address with malicious addr
23
24 .text
25 main:
26 # Simulate calling a function with attacker-controlled data
27 la a0, attacker_payload # load address of attacker payload
28 jal ra, process_user_input # call vulnerable function
29
30 # Normal exit (we won't reach here due to overflow)
31 li a7, 10
32 ecall
33
34 #
35 # process_user_input(char *input):
36 # Simulates a vulnerable function that processes user input without bounds checking.
37 # In real code, this might be a function that reads network data, parses files,
38 # or handles user input - all common sources of buffer overflow vulnerabilities.
39 #
40 # Stack layout (32-byte frame):
41 # sp+0 to sp+15: buffer (16 bytes, 4 words) - local storage
42 # sp+16 to sp+27: unused space
43 # sp+28 to sp+31: saved return address (ra)
44 #
45 process_user_input:

```

Figure 3: CREATOR main interface.

Access

Visit <https://creatorsim.github.io/creator> to use CREATOR online.

Features

- **Multi-Architecture Support:** Work with RISC-V, MIPS, Z80, and custom architectures.
- **Integrated Code Editor:** Syntax highlighting, IntelliSense, and code navigation.
- **Simulator:** Step through code, set breakpoints, and inspect memory/registers.
- **Modular Assemblers:** Support for multiple assemblers like CREATOR Assembler and RASM.
- **User-Friendly Interface:** Intuitive layout with architecture selection, code editor, and simulator panels.

User Interface

The CREATOR web interface is designed for efficiency and ease of use. This guide covers all UI components and their functions.

CREATOR uses a familiar global menu bar at the top of the window for accessing various features and settings, which change based on the current view. There are four main views: Architecture Select, Editor, Simulator, and Architecture. To change between the views, use the “View” menu in the top-left corner.

Architecture Select View

The Architecture Select view is the initial screen you see when you open CREATOR. It allows you to choose the processor architecture you want to work with. You can select from a list of predefined architectures or load a custom architecture YAML file.

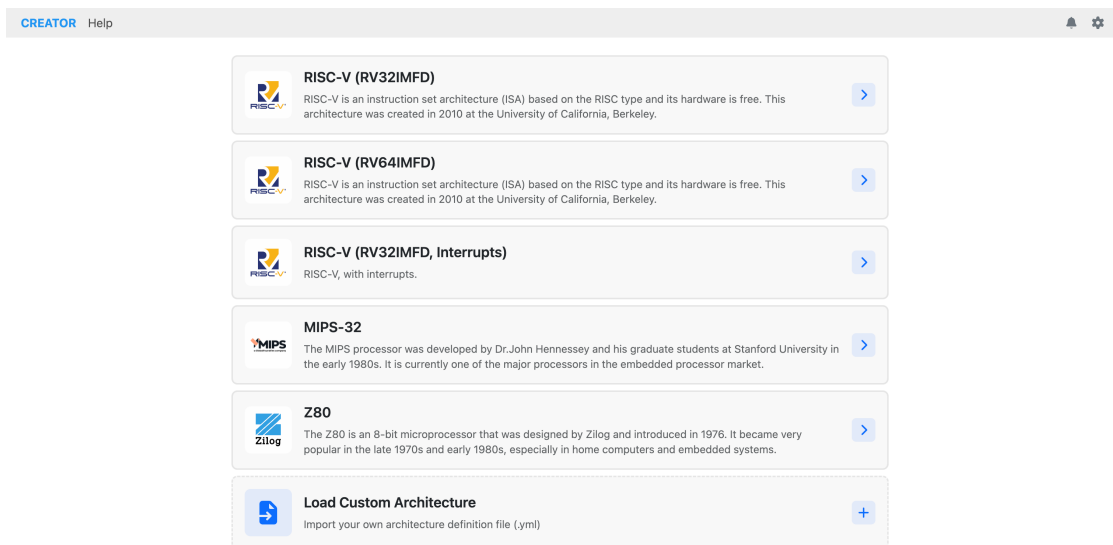


Figure 4: Architecture selection view for choosing processor architecture.

Editor View

CREATOR features a powerful code editor based on the Monaco Editor (the same editor used in VS Code). The editor supports syntax highlighting, IntelliSense, line numbers, breakpoints, and more. For specific editor features, refer to the Editor Features chapter.

```

CREATOR View File Library Help  Assemble Assemble & Run Vim: off
1 # This example demonstrates a classic buffer overflow attack in RISC-V assembly.
2 # In real-world software, buffer overflows can occur when copying data without
3 # proper bounds checking, allowing attackers to overwrite critical data like
4 # return addresses and hijack program execution.
5 # To visualize the exploit, go to the Memory tab in the simulator, click on
6 # the Stack segment, and observe how the stack changes during execution.
7
8 .data
9 .align 4
10 # Simulated attacker-controlled input: This represents data that an attacker
11 # might provide, such as overly long user input or malicious network data.
12 # The payload is crafted to overflow the buffer and overwrite the saved return
13 # address with the address of malicious code.
14 attacker_payload:
15     .word 0xCAFECAFE # filler data (padding to reach return address)
16     .word 0xCAFECAFE
17     .word 0xCAFECAFE
18     .word 0xCAFECAFE
19     .word 0xCAFECAFE
20     .word 0xCAFECAFE
21     .word 0xCAFECAFE # 7 words * 4 bytes = 28 bytes to reach saved ra
22     .word malicious # overwrites saved return address with malicious addr
23
24 .text
25 main:
26     # Simulate calling a function with attacker-controlled data
27     la a0, attacker_payload # load address of attacker payload
28     jal ra, process_user_input # call vulnerable function
29
30     # Normal exit (we won't reach here due to overflow)
31     li a7, 10
32     ecall
33
34 #
35 # process_user_input(char *input):
36 # Simulates a vulnerable function that processes user input without bounds checking.
37 # In real code, this might be a function that reads network data, parses files,
38 # or handles user input - all common sources of buffer overflow vulnerabilities.
39 #
40 # Stack layout (32-byte frame):
41 # sp+0 to sp+15: buffer (16 bytes, 4 words) - local storage
42 # sp+16 to sp+27: unused space
43 # sp+28 to sp+31: saved return address (ra)
44 #
45 process_user_input:

```

Figure 5: Default view of the code editor with syntax highlighting.

Editor Menu Actions

When in the editor view, the menu bar provides the following exclusive actions: ##### File

- **New File...:** Clear editor and start fresh
- **Open File...:** Load file from disk
- **Save As:** Download current code
- **Examples...:** Load example code
- **Get Code as URI:** Generate shareable URL

Library

- **Load Library...:** Load assembly libraries
- **Remove Library...:** Remove the loaded library
- **Library Tags:** View tags from the loaded library

Simulator View

The simulator view is divided into two columns: the left column contains the loaded instructions, while the right column contains tabs for execution control, registers, memory, and statistics.

```

CREATOR View File Library Help  Assemble Assemble & Run Vim: off
1 # This example demonstrates a classic buffer overflow attack in RISC-V assembly.
2 # In real-world software, buffer overflows can occur when copying data without
3 # proper bounds checking, allowing attackers to overwrite critical data like
4 # return addresses and hijack program execution.
5 # To visualize the exploit, go to the Memory tab in the simulator, click on
6 # the Stack segment, and observe how the stack changes during execution.
7
8 .data
9 .align 4
10 # Simulated attacker-controlled input: This represents data that an attacker
11 # might provide, such as overly long user input or malicious network data.
12 # The payload is crafted to overflow the buffer and overwrite the saved return
13 # address with the address of malicious code.
14 attacker_payload:
15     .word 0xCAFECAFE # filler data (padding to reach return address)
16     .word 0xCAFECAFE
17     .word 0xCAFECAFE
18     .word 0xCAFECAFE
19     .word 0xCAFECAFE
20     .word 0xCAFECAFE
21     .word 0xCAFECAFE # 7 words * 4 bytes = 28 bytes to reach saved ra
22     .word malicious # overwrites saved return address with malicious addr
23
24 .text
25 main:
26     # Simulate calling a function with attacker-controlled data
27     la a0, attacker_payload # load address of attacker payload
28     jal ra, process_user_input # call vulnerable function
29
30     # Normal exit (we won't reach here due to overflow)
31     li a7, 10
32     ecall
33
34 #
35 # process_user_input(char *input):
36 # Simulates a vulnerable function that processes user input without bounds checking.
37 # In real code, this might be a function that reads network data, parses files,
38 # or handles user input - all common sources of buffer overflow vulnerabilities.
39 #
40 # Stack layout (32-byte frame):
41 # sp+0 to sp+15: buffer (16 bytes, 4 words) - local storage
42 # sp+16 to sp+27: unused space
43 # sp+28 to sp+31: saved return address (ra)
44 #
45 process_user_input:

```

Figure 6: Default simulator panel showing execution controls and tabs.

Left Column: Instruction List

The left column displays the list of loaded instructions in a scrollable panel. Each instruction is shown with its address, user representation (which may include pseudo-instructions), and the underlying assembled instruction.

Right Column: Simulator Tabs

1. Registers Tab The Registers tab displays the register bank(s) for the loaded architecture. You can view values in hexadecimal (the default), decimal (signed or unsigned) Clicking on a register opens a modal that shows even more display options, including binary, char, and IEEE 754 formats. This modal also allows you to edit the register value directly.

2. Memory Tab The Memory tab provides a full-featured hex editor. You can navigate to specific addresses, jump to memory sections (data, code, stack, heap), and toggle the tag display for easier debugging. The tag display shows the name of the variable or section associated with each memory address, if available. Hints are also shown for memory locations that have been tagged with type information. These addresses are highlighted in a different color for easy identification.

The hex editor also provides a memory layout diagram to help visualize different memory regions and their purposes.

To jump to a specific address, use the “Go to Address” input field. You can also quickly navigate

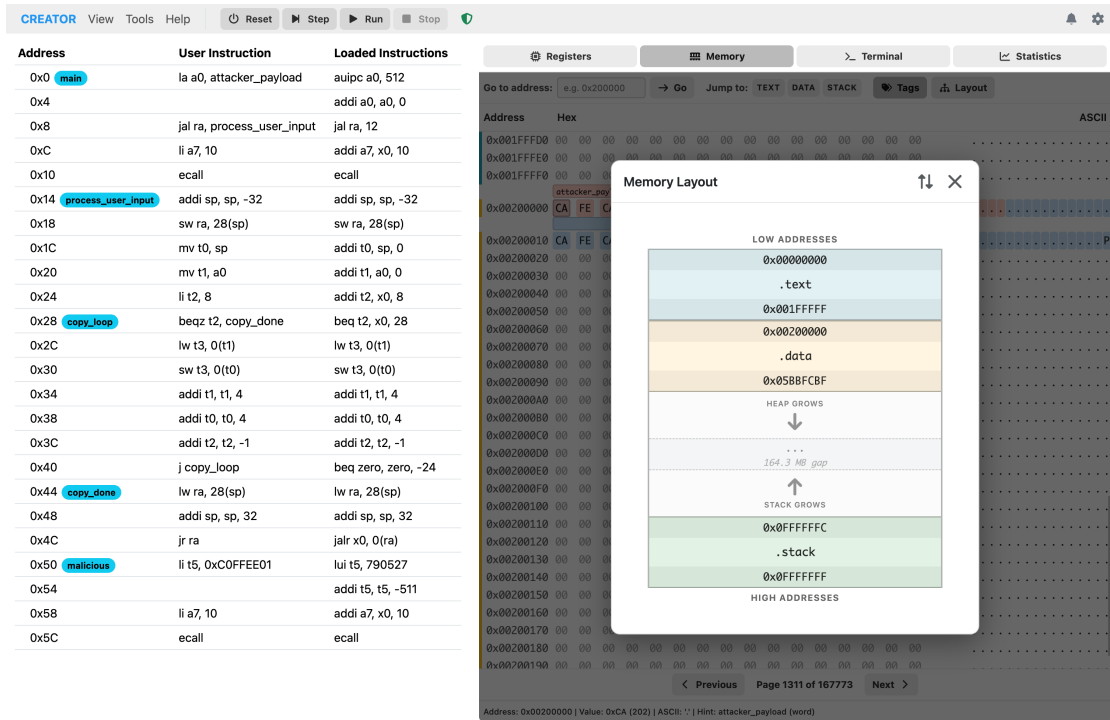


Figure 9: Memory layout diagram showing different memory regions.

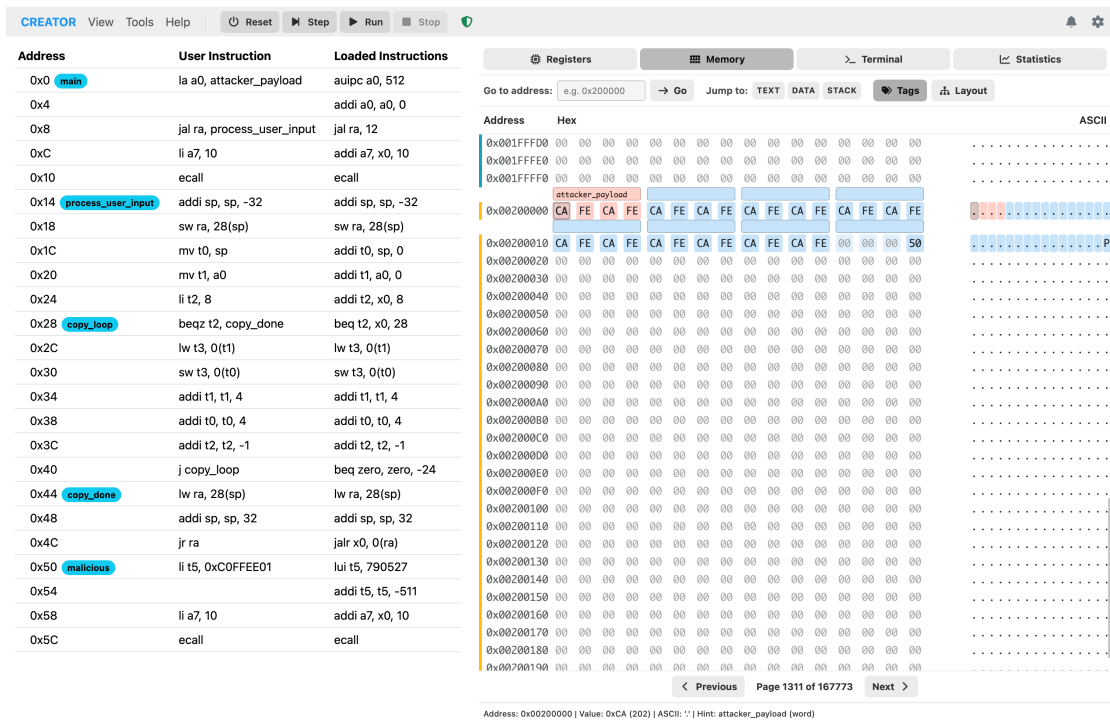


Figure 10: Memory viewer focused on data section.

editing mode allows you to modify memory on-the-fly during program execution or while paused at a breakpoint. You can edit multiple bytes in a row, simply by typing the new values consecutively.

3. Terminal Tab The terminal tab provides an interface for program input and output, simulating a console environment.

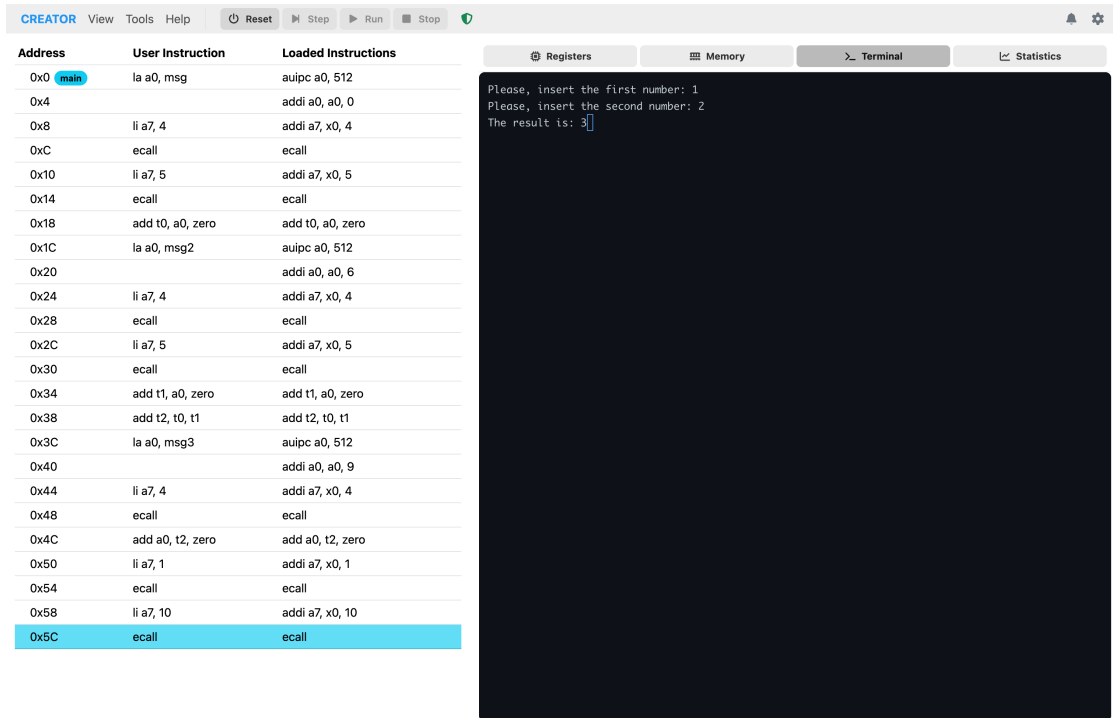


Figure 11: Terminal tab showing a simple sum program interaction.

4. Statistics Tab The Statistics tab shows execution metrics including the number of instructions executed, clock cycles, CPI (Cycles Per Instruction), and simulated execution time.

Sentinel

CREATOR includes a Sentinel feature that monitors the execution status of your program. It provides feedback on whether the parameter passing conventions are being followed correctly. The sentinel button changes color based on the status: - **Green (OK)**: All parameters passed correctly - **Red (Error)**: Parameter passing conventions violated

Architecture View

The architecture panel provides detailed information about the currently loaded architecture, including registers, instructions, directives, and pseudo-instructions. The left sidebar contains general architecture information such as the name, word size, endianness, and other relevant details.

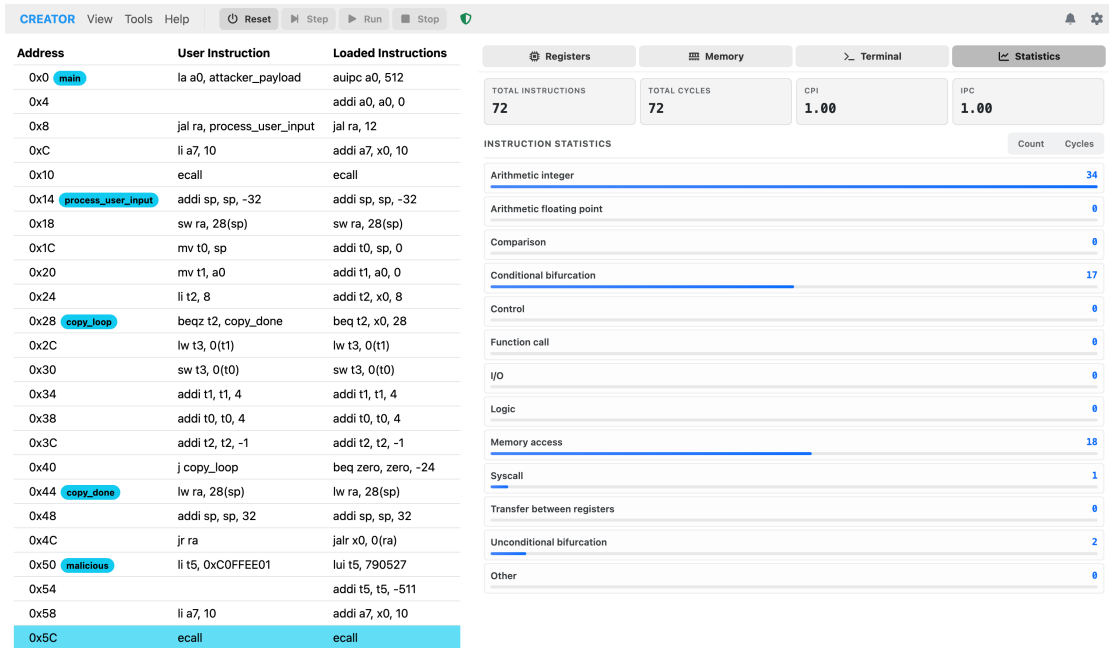


Figure 12: Statistics tab displaying execution metrics and performance data.

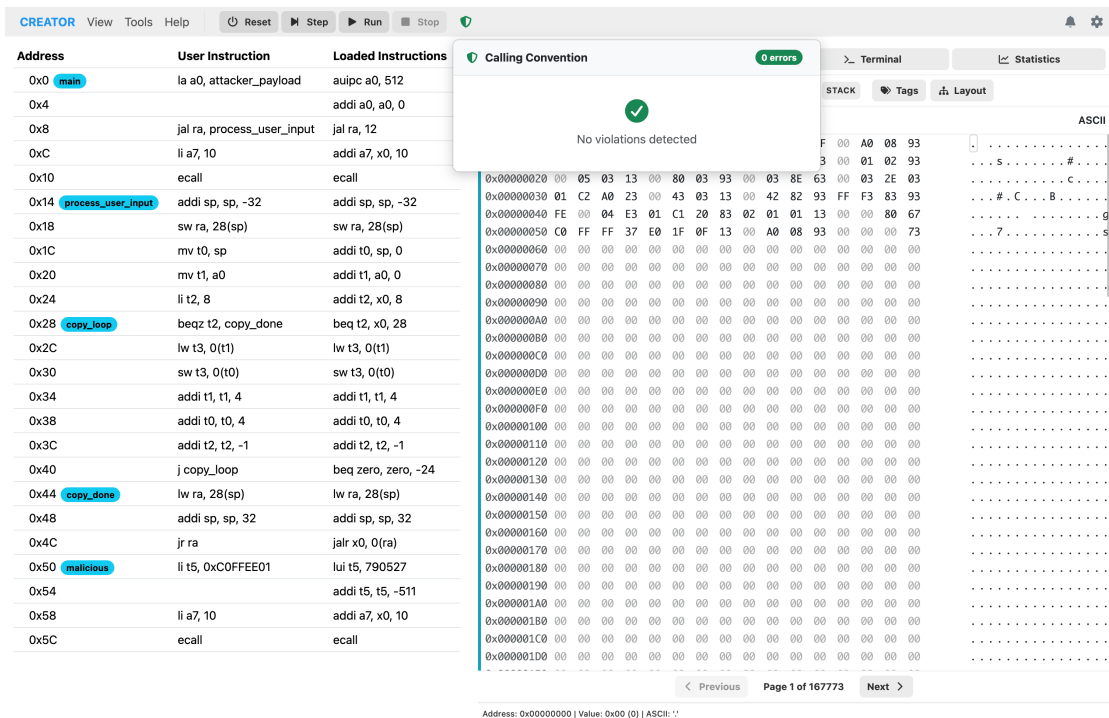


Figure 13: Simulator panel with sentinel status OK, indicating successful execution.

Architecture Instructions

The instructions section lists all supported assembly instructions for the selected architecture, along with their syntax, help, and encoding details. The diagrams are dynamically generated based on the

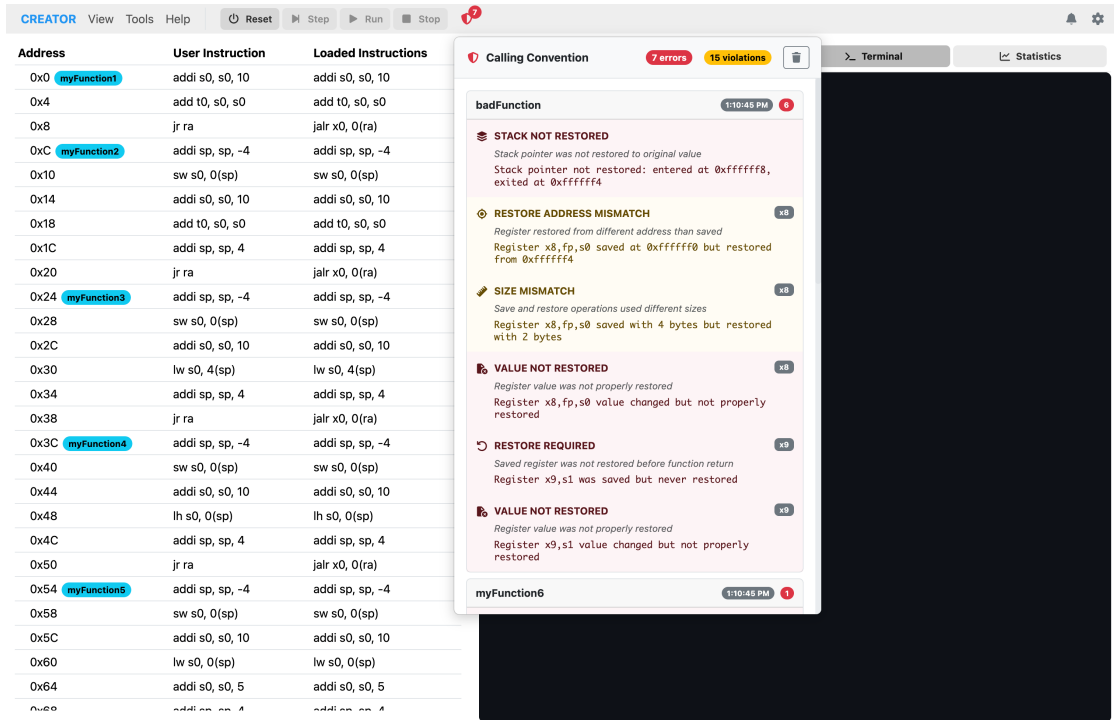


Figure 14: Simulator panel with sentinel status Error, indicating a parameter passing violation.

architecture YAML definition.

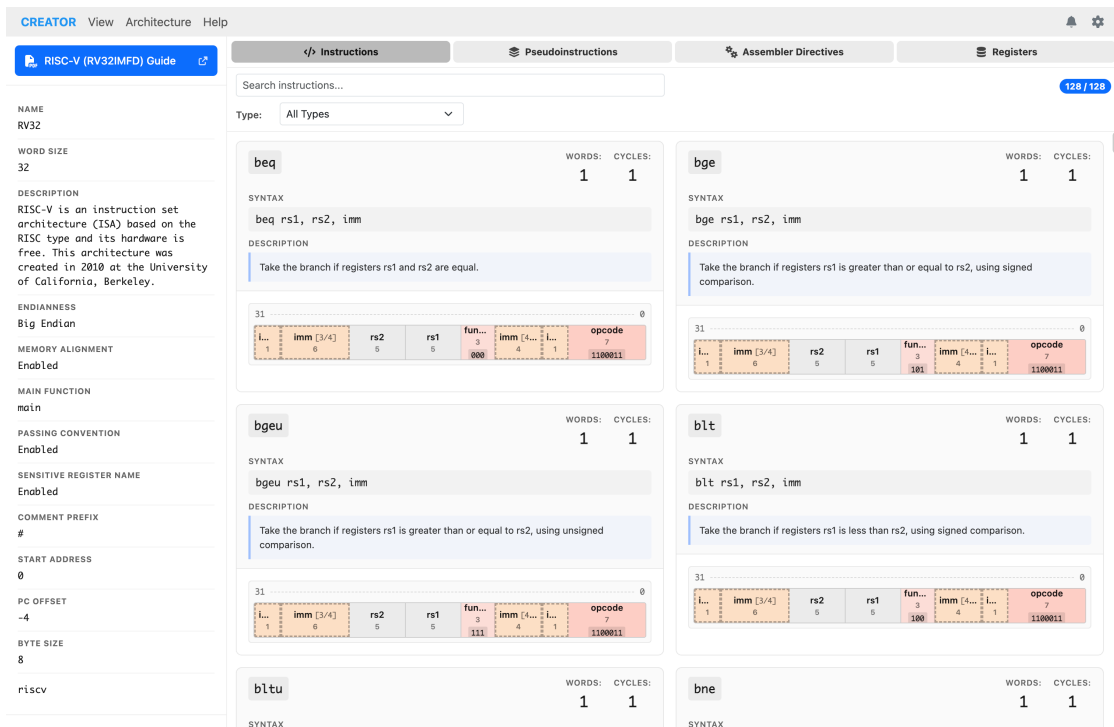


Figure 15: List of supported assembly instructions.

Architecture Pseudo-Instructions

The pseudo-instructions section displays all pseudo-instructions available for the architecture. Pseudo-instructions are higher-level assembly commands that expand into one or more real instructions during assembly.

Name	Syntax	Expands To
<code>beqz</code>	<code>beqz rs1, off</code>	<code>beq rs1, x0, off;</code>
<code>bgez</code>	<code>bgez rs1, off</code>	<code>bge reg1, x0, off;</code>
<code>bgt</code>	<code>bgt rs1, rs2, off</code>	<code>blt rs2, rs1, off;</code>
<code>bgtu</code>	<code>bgtu rs1, rs2, off</code>	<code>bltu rs2, rs1, off;</code>
<code>bgtz</code>	<code>bgtz rs1, off</code>	<code>bgt rs1, x0, off;</code>
<code>ble</code>	<code>ble rs1, rs2, off</code>	<code>bge rs2, rs1, off;</code>
<code>bleu</code>	<code>bleu rs1, rs2, off</code>	<code>bgeu rs2, rs1, off;</code>
<code>blez</code>	<code>blez rs1, off</code>	<code>ble x0, rs1, off;</code>
<code>bltz</code>	<code>bltz rs1, off</code>	<code>blt rs1, x0, off;</code>
<code>bnez</code>	<code>bnez rs1, off</code>	<code>bne rs1, x0, off;</code>
<code>j</code>	<code>j off</code>	<code>beq zero, zero, off;</code>
<code>jalr</code>	<code>jalr rs</code>	<code>jalr x1, 0(rs);</code>
<code>jr</code>	<code>jr rs</code>	<code>jalr x0, 0(rs);</code>
<code>la</code>	<code>la rd, addr</code>	<pre>no_ret_op{ tmp = Field.2(31,0).int; tmp_pc_offset = (reg_pc - 4) & 0xFFF; tmp_low = tmp & 0x00000FFF; tmp_hi = tmp >> 12; }; auipc rd, op(tmp_hi); addi rd, rd, op[tmp_low - (tmp_pc_offset)];</pre>
<code>lscv</code>		<pre>no_ret_op{ tmp = Field.2(31,0).int; tmp_low = tmp & 0x00000FFF; tmp_low -= tmp_low > 0x7FF ? 0x1000 : 0; tmp_hi = (tmp - tmp_low) >>> 12; };</pre>

Figure 16: Pseudo-instructions that expand to multiple real instructions.

Architecture Directives

The directives section shows all assembler directives supported by the architecture, along with their syntax and descriptions.

Architecture Registers

The registers section provides a comprehensive list of all registers defined in the architecture, including their names, descriptions, and types.

Settings Menu

The setting menu is always accessible from the top-right corner of the interface. It provides options to customize the appearance and behavior of the editor and simulator.

The settings menu allows you to switch from light and dark mode. You can also adjust editor preferences and customize keyboard shortcuts.

Name	Action	Size
.data	data_segment	
.text	code_segment	
.bss	global_symbol	
.zero	space	1
.space	space	1
.align	align	
.balign	balign	
.globl	global_symbol	
.string	ascii_null_end	
.asciz	ascii_null_end	
.ascii	ascii_not_null_end	
.byte	byte	1
.half	half_word	2
.word	word	4
.dword	double_word	8
.float	float	4
.double	double	8

Figure 17: Assembler directives available for the architecture.

Control registers (1 registers)

- PC** #0
 - Bits: 32
 - Default: 0x00000000
 - Buttons: read, write, program_counter

Integer registers (32 registers)

- x0 / zero** #0
 - Bits: 32
 - Default: 0x00000000
 - Buttons: read, ignore_write
- x1 / ra** #1
 - Bits: 32
 - Default: 0xFFFFFFFF
 - Buttons: read, write
- x2 / sp** #2
 - Bits: 32
 - Default: 0x01999999
 - Buttons: read, write, stack_pointer
- x3 / gp** #3
 - Bits: 32
 - Default: 0x00000000
 - Buttons: read, write, global_pointer
- x4 / tp** #4
 - Bits: 32
 - Default: 0x00000000
 - Buttons: read, write
- x5 / t0** #5
 - Bits: 32
 - Default: 0x00000000
 - Buttons: read, write
- x6 / t1** #6
 - Bits: 32
 - Default: 0x00000000
 - Buttons: read, write
- x7 / t2** #7
 - Bits: 32
 - Default: 0x00000000
 - Buttons: read, write
- x8 / fp / s0** #8
 - Bits: 32
 - Default: 0x00000000
 - Buttons: read, write

Figure 18: Architecture panel showing available registers for the selected processor.

CREATOR Remote Laboratory

CREATOR’s Remote Laboratory allows students to execute their programs in remote ESP32 hardware provided by their teachers.

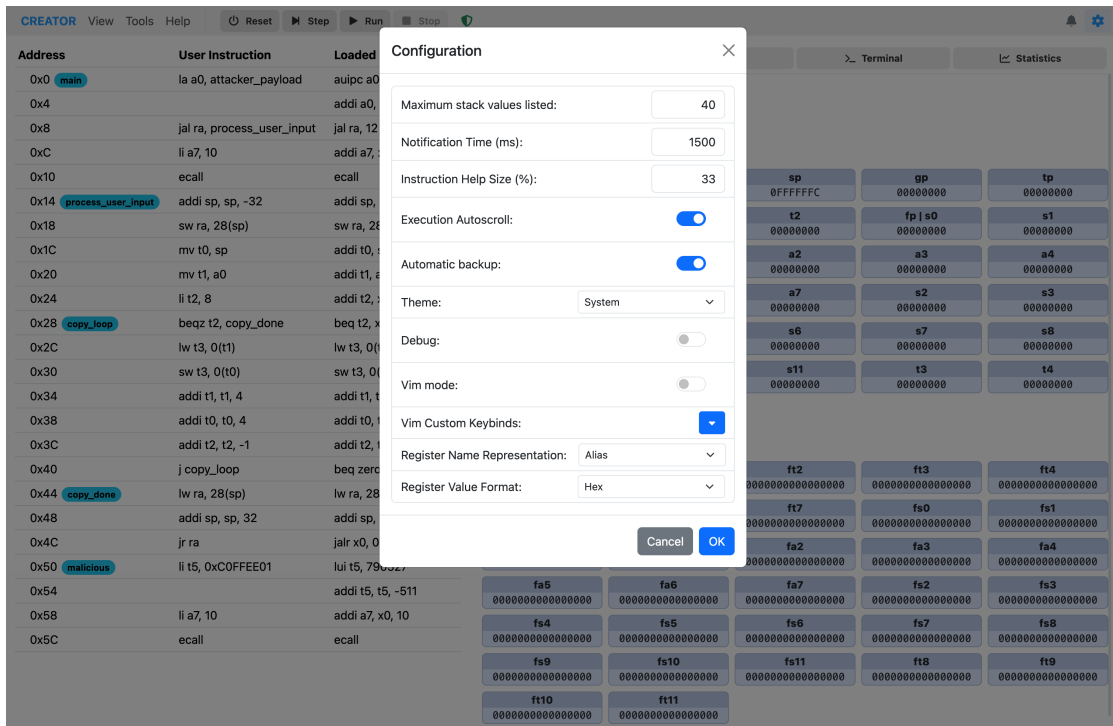


Figure 19: Settings menu drop-down showing theme selection and other options



CREATOR 6.0.x does not support keyboard (STDIN) inputs.



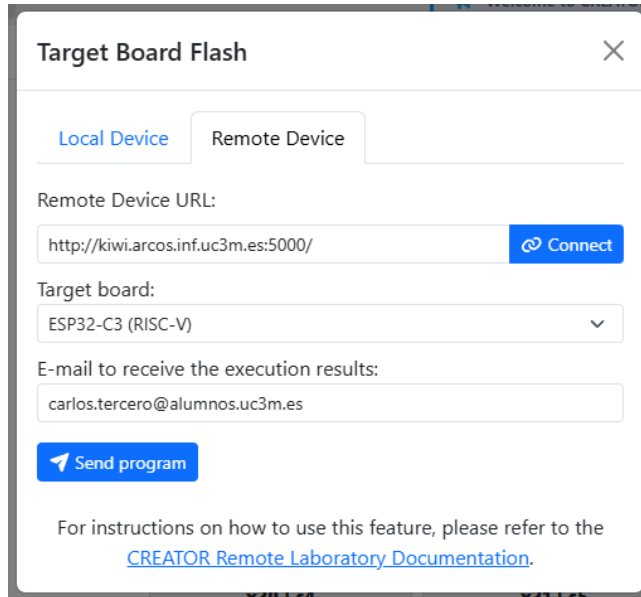
If you want to deploy your own remote laboratory, see [Setting up the Remote Laboratory](#).

User Interface

The Remote Device Target Flash menu can be accessed from *Tools* → *Flash* → *Remote Device* in the simulator view.

1. Connect to the Remote Device URL where the server is deployed, e.g.
`http://remote.arcos.inf.uc3m.es:5000`.
2. Select one of the available board types that the server supports
3. Enter your e-mail address to receive the execution results
4. Execute your program by using the *Send program* button.

The status of your program will be displayed. You can cancel the execution by using the *Cancel last program* button.



Target Board Flash [X]

Local Device | Remote Device

Remote Device URL:
 [Connect](#)

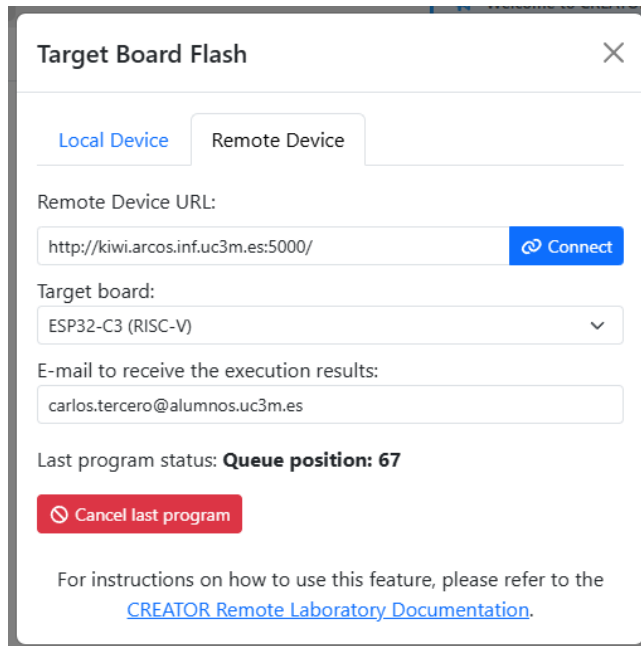
Target board:

E-mail to receive the execution results:

[Send program](#)

For instructions on how to use this feature, please refer to the [CREATOR Remote Laboratory Documentation](#).

Figure 20: Remote Device Target



Target Board Flash [X]

Local Device | Remote Device

Remote Device URL:
 [Connect](#)

Target board:

E-mail to receive the execution results:

Last program status: **Queue position: 67**

[Cancel last program](#)

For instructions on how to use this feature, please refer to the [CREATOR Remote Laboratory Documentation](#).

Figure 21: Remote UI (queued)

Editor Features

The CREATOR web editor is based on Monaco Editor, the same editor that powers Visual Studio Code.

Syntax Highlighting

Assembly language syntax is highlighted for better readability. This supports any architecture defined in CREATOR and requires no additional configuration.

Developers can extend or override the default syntax highlighting by creating their own language definitions. See the Development chapter for details.

Auto-Completion (IntelliSense)

As you type, the editor suggests completions for instructions, registers, and labels. These suggestions adapt to the currently selected architecture.

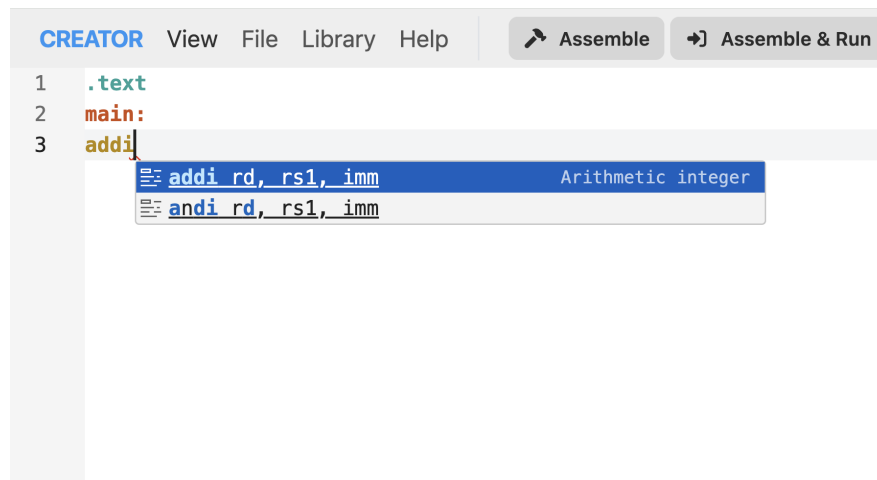


Figure 22: Auto-completion suggestions for RISC-V instructions.

Help Tooltips

Hover over instructions to see detailed help tooltips, including syntax, description, and usage examples.

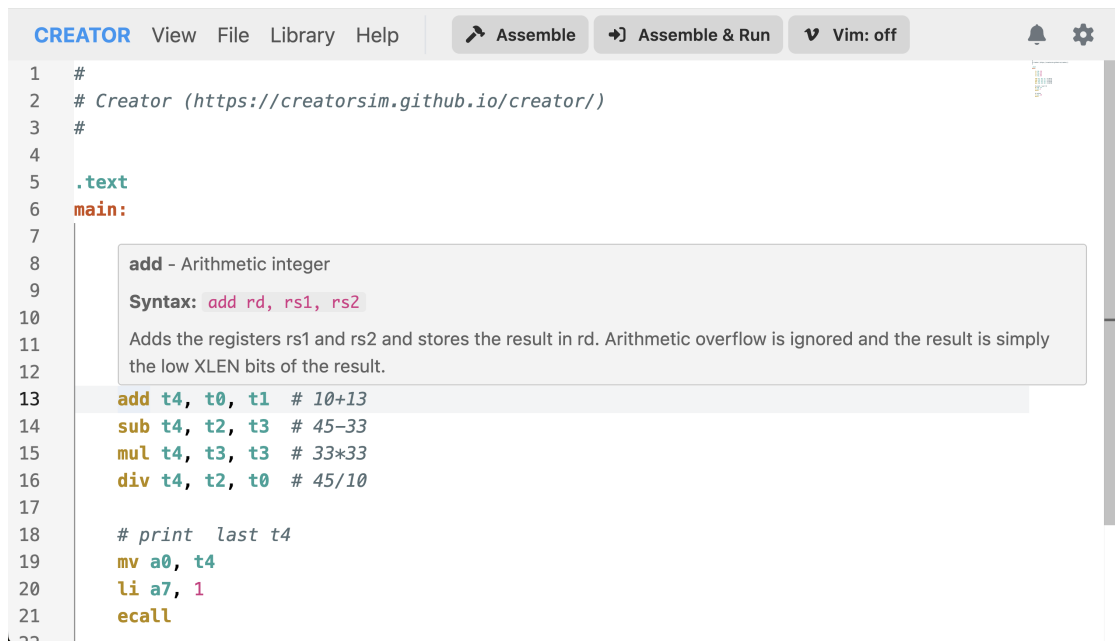
Go to Definition/References

Right-click a label and select “Go to Definition” to jump to its declaration. Right-click and select “Find All References” to see all usages of that label in your code.

Code Comments

Single-Line Comments

Comments are architecture dependent. For RISC-V and MIPS, use # for single-line comments. The comment prefix for any given architecture can be consulted in the “Architecture View” chapter.

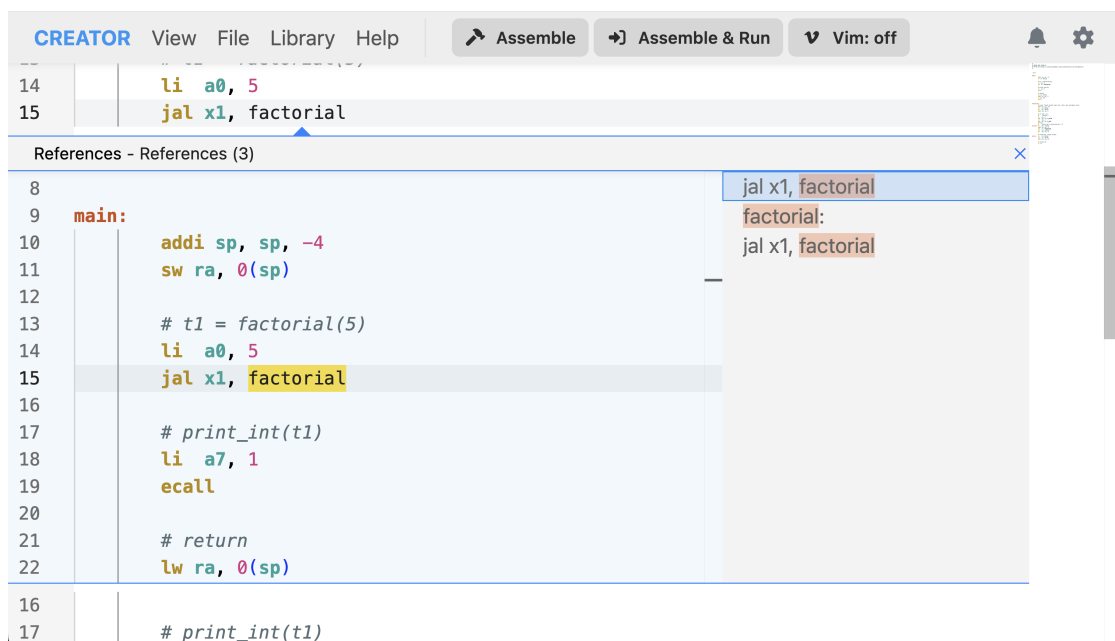


```

1 #
2 # Creator (https://creatorsim.github.io/creator/)
3 #
4
5 .text
6 main:
7
8   add - Arithmetic integer
9   Syntax: add rd, rs1, rs2
10  Adds the registers rs1 and rs2 and stores the result in rd. Arithmetic overflow is ignored and the result is simply
11  the low XLEN bits of the result.
12
13  add t4, t0, t1 # 10+13
14  sub t4, t2, t3 # 45-33
15  mul t4, t3, t3 # 33*33
16  div t4, t2, t0 # 45/10
17
18  # print last t4
19  mv a0, t4
20  li a7, 1
21  ecall
22

```

Figure 23: Help tooltip for the ADD instruction in RISC-V.



```

14  li a0, 5
15  jal x1, factorial

```

References - References (3)

```

8
9  main:
10  addi sp, sp, -4
11  sw ra, 0(sp)
12
13  # t1 = factorial(5)
14  li a0, 5
15  jal x1, factorial
16
17  # print_int(t1)
18  li a7, 1
19  ecall
20
21  # return
22  lw ra, 0(sp)

```

Figure 24: Finding all references to a label in the code.

Minimap

The minimap shows a bird's-eye view of your code: - Located on the right side of the editor - Shows entire file structure - Click to jump to sections - Highlights current viewport

Error and Warning Indicators

In supported architectures, the editor provides real-time error and warning indicators as you type. These errors are displayed as squiggly lines under the relevant code sections.

Common errors include: - Syntax errors - Unknown instructions - Invalid operands - Missing labels

Hover over the squiggly lines to see detailed error messages.

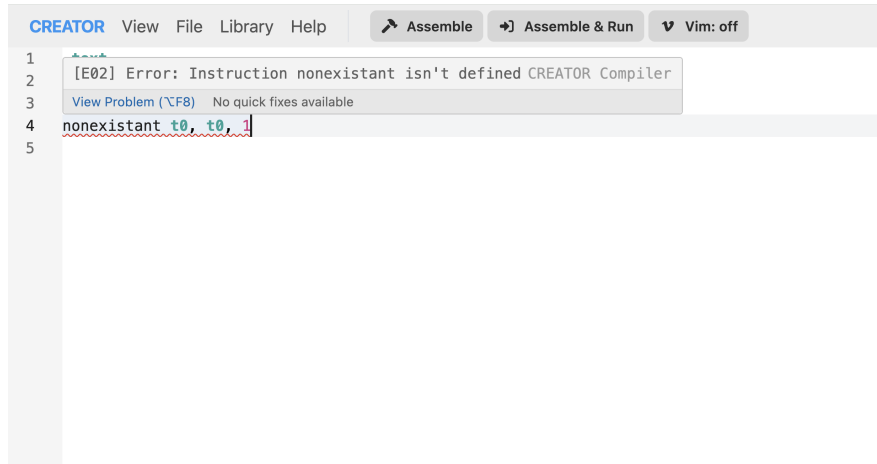


Figure 25: Error and warning indicators in the editor.

Vim Mode

Advanced users can enable Vim keybindings by clicking the “Vim” button in the editor toolbar. This activates Vim mode, allowing users to navigate and edit code using Vim commands. Custom keybinding can also be configured in the settings.

CREATOR Gateway

CREATOR supports the execution of RISC-V programs in real hardware devices.



We also support our predefined RISC-V system calls

Supported devices

CREATOR supports Espressif ESP32 development boards and RISC-V SBCs.

Espressif ESP32

Espressif’s family of ESP32 MCUs.

```

7
8     li t0, 10
9     li t1, 13
10    li t2, 45
11    li t3, 33
12
13    add t4, t0, t1 # 10+13
14    sub t4, t2, t3 # 45-33
15    mul t4, t3, t3 # 33*33
16    div t4, t2, t0 # 45/10
17
18    # print last t4
19    mv a0, t4
20    li a7, 1
21    ecall
22
23    # return
24    li a7, 10
25    ecall
26
27
--VISUAL BLOCK--

```

Figure 26: Vim mode enabled in the editor.

- esp32c3
 - ESP32-C3-DevKitC-02 (includes JTAG)
 - ESP32-C3-DevKitM-1 (no JTAG detected)
- esp32c6
 - ESP32-C6-DevKitC-1 (JTAG + port included)
 - ESP32-C6-DevKitM-1 (JTAG + port included)
- esp32h2
 - ESP32-H2-DevKitM-1 (JTAG + port)

These use the creator-gateway-esp32.

Single-Board Computers

RISC-V SBC boards with Linux that can run SSH and GDBGUI. At the moment, SBC RISC-V boards with Ubuntu 24.04.3 for RISC-V fulfill these requirements.

- OrangePi RV2: 8 RISC-V cores, Wi-Fi and Bluetooth connection
- Nezha D1-H 64 bit RISC-V: Single-core RISC-V64. It does not offer Wi-Fi connection or a GUI

These use the creator-gateway-sbc.

Executing the ESP32 gateway

Docker execution

This is the recommended way of executing the gateway on Windows, Linux, or macOS.

For more information, see the IDF documentation.

Windows

1. Install Docker Desktop
2. Connect your device and check which port it belongs to. You can do this with the `mode` terminal command, or in the Device Manager. The default port is COM3.
3. Set up the Remote Serial Port:
4. Download and unzip `esptool`
5. Run `esp_ffc2217_server` in the device's port (e.g. COM3):

```
1 powershell> esp_ffc2217_server -v -p 4000 COM3
2
```

6. Run the container:

```
1 docker run --rm --name creator-gateway-esp32 -it \
2     --init \
3     -p 8080:8080 -p 5000:5000 \
4     --add-host=host.docker.internal:host-gateway \
5     creatorsim/creator-gateway-esp32:latest
6
```



You can also use a Docker compose file (`compose.yaml`):

1. Create the following `compose.yaml` file:

```

1 services:
2   creator-gateway-esp32:
3     image: creatorsim/creator-gateway-esp32:latest
4     ports:
5       - "8080:8080" # gateway
6       - "5000:5000" # gdbgui
7     stdin_open: true
8     tty: true
9     init: true
10    # for debug
11    network_mode: bridge
12    extra_hosts:
13      - "host.docker.internal:host-gateway"

```

2. Deploy the docker compose in the directory of the YAML file:

```
1 docker compose up
```

Take into account that `docker compose up` is not interactive, therefore the program won't be able to read the keyboard inputs. You can run `docker compose up -d` and then attach to the specific container (check its name/id with `docker ps`) with `docker attach <container>`.

Linux/macOS

1. Install Docker engine (or Docker Desktop)
2. Connect your device and check which port it belongs to. It typically resides in `/dev/`, e.g. `/dev/ttyUSB0`. You can quickly check it with `ls /dev/ttyUSB*` (Linux) or `ls /dev/cu.usbserial-*` (macOS).
3. Run the container:

```

1 docker run --rm --name creator-gateway-esp32 -it \
2   --init \
3   -p 8080:8080 -p 5000:5000 \
4   --device=/dev/ttyUSB0 \
5   --add-host=host.docker.internal:host-gateway \
6   creatorsim/creator-gateway-esp32
7

```



You can also use a Docker compose file (`compose.yaml`):

1. Create the following `compose.yaml` file:

```
1 services:
2   creator-gateway-esp32:
3     image: creatorsim/creator-gateway-esp32:latest
4     ports:
5       - "8080:8080" # gateway
6       - "5000:5000" # gdbgui
7     stdin_open: true
8     tty: true
9     init: true
10    devices:
11      - /dev/ttyUSB0 # device port
12      # for debug
13    network_mode: bridge
14    extra_hosts:
15      - "host.docker.internal:host-gateway"
```

2. Deploy the docker compose in the directory of the YAML file:

```
1 docker compose up
```

Take into account that `docker compose up` is not interactive, therefore the program won't be able to read the keyboard inputs. You can run `docker compose up -d` and then attach to the specific container (check its name/id with `docker ps`) with `docker attach <container>`.

Setting up the debugger The debugger is only available in boards with JTAG, and both USB and SERIAL ports must be connected to the computer.



For boards without the secondary port on the board, but with JTAG support, you can wire a USB-to_Dip as such:

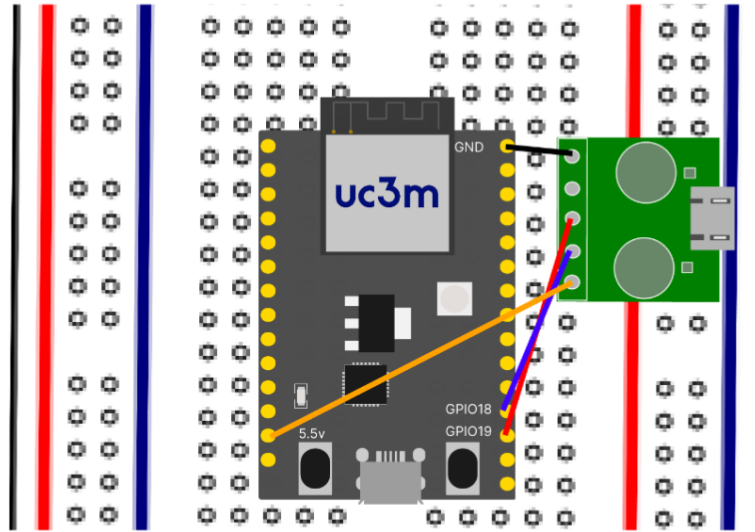


Figure 27: JTAG connection.

Linux/macOS

1. Setup OpenOCD
2. Download OpenOCD with ESP32 JTAG support v0.12.0-esp32-20241016 (for your OS and architecture) and unzip it
3. Add the bin/ folder to your PATH, e.g.:

```
1 export PATH="/full/path/to/openocd-esp32/bin:$PATH"
```

4. Set the OPENOCD_SCRIPTS environment variable:

```
1 export OPENOCD_SCRIPTS="/full/path/to/openocd-esp32/share/openocd/scripts"
```

5. Execute the `openocd_start.sh` script (inside the `openocd_scripts` folder in our driver) with the type of device (e.g. `esp32c3`)

```
1 ./openocd_start.sh esp32c3
```

6. After the container confirms that GDBGUI is up and running, access the web interface at <http://localhost:5000>

Windows

1. Install and setup Zadig
2. List all the devices in `Options > List All Devices` and select `USB Jtag/serial debug unit (Interface 2)`

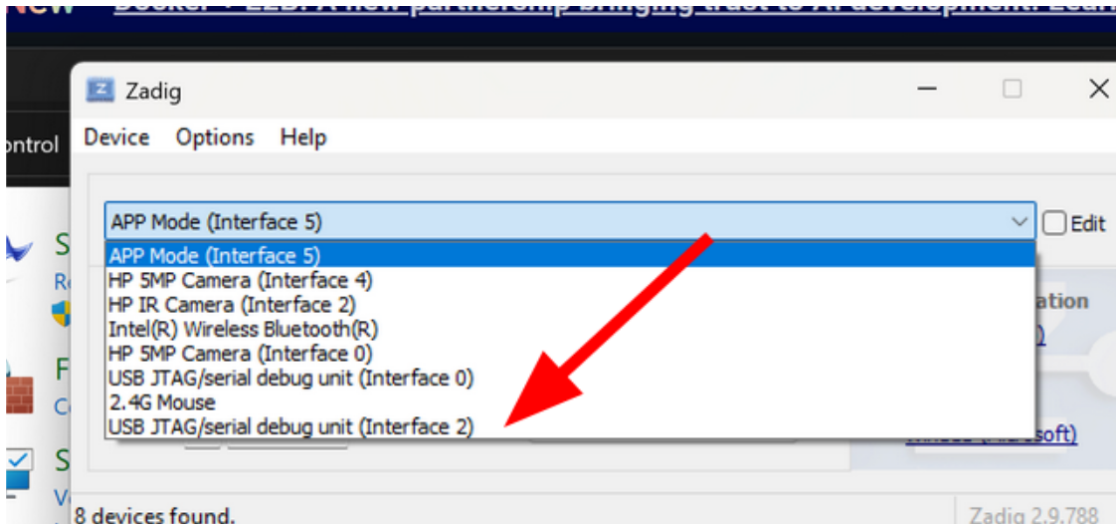


Figure 28: Zadig set device.

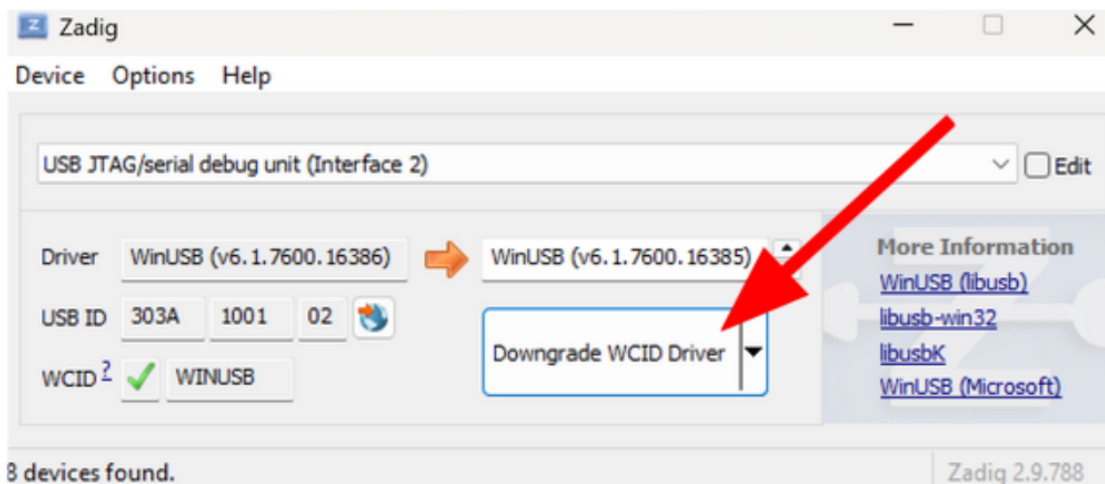


Figure 29: Zadig downgrade driver.

3. Downgrade the driver:
4. Setup OpenOCD
5. Download OpenOCD with ESP32 JTAG support v0.12.0-esp32-20241016 (for your OS and architecture) and unzip it.
6. Add the bin\ folder to your PATH, e.g.:


```
1 set PATH=%PATH%;<openocd-esp32 path>\bin\
```
7. Execute the openocd_start.bat script (inside the openocd_scripts folder in our driver) with the type of device (e.g. esp32c3)


```
1 \openocd_start.bat esp32c3
```
8. After the container confirms that GDBGUI is up and running, access the web interface at <http://localhost:5000>

Native execution (Linux-only)

You can run the gateway natively on your Linux device.

1. Install Python 3.9

- With uv:

```
1 uv python install 3.9
```

- In Ubuntu:

```
1 sudo apt install software-properties-common sudo add-apt-repository ppa:deadsnakes/ppa
  sudo apt install python3.9
```

2. Install the ESP-IDF framework v5.3.2

- Follow the instructions from Espressif's documentation.
- To ensure Python 3.9 is used for the installation, first create a virtual environment in `~/.espressif/python_env/idf5.3_py3.9_en`, and activate it, before executing the `install.sh` script.

```
1 python3.9 -m venv ~/.espressif/python_env/idf5.3_py3.9_en source ~/.espressif/
  python_env/idf5.3_py3.9_env/bin/activate
```

3. Download and unzip the ESP32 gateway

4. Install the python dependencies

5. Use the `install.sh` script from ESP-IDF:

```
1 /path/tp/esp-idf-v5.3.2/install.sh
```

6. Install the Python dependencies with pip (move to the downloaded folder):

```
1 pip3 install -r requirements.txt
```

7. Load the ESP-IDF environment variables (`export.sh`)

8. Execute the gateway web service:

```
1 python3 gateway.py
```

Setting up the debugger You must set up **ports permissions** for the JTAG. Your user must be in the `plugdev` and `dialout` groups (in Ubuntu/Debian/Fedora), or `uucp` (in Arch Linux).

You can add yourself to the group with `usermod`, e.g.:

```
1 sudo usermod -a -G dialout $USER
2 sudo usermod -a -G plugdev $USER
```

Another error might occur: `gdb_exception_error - libusb_bulk_write error: LIBUSB_ERROR_NO_DEVICE`. This problem happens because the user doesn't have permission to write to the JTAG USB device, located in `/dev/bus/usb/003/XXX` (where XXX is a pseudo-random number).

You can check this by doing:

```
1 ls -lah /dev/bus/usb/003
```

And an example of the output might be:

```
1 total 0
2 drwxr-xr-x 2 root root 180 Oct 1 11:03 .
3 drwxr-xr-x 6 root root 120 Oct 1 10:36 ..
4 crw-rw-r-- 1 root root 189, 256 Oct 1 10:41 001
5 ...
6 crw-rw-r-- 1 root root 189, 256 Oct 1 10:41 022
```

You can see the user and group are root.

To change this, we can configure udev so that, when it mounts the JTAG device it gives it the group permissions it typically gives to all other devices (`uucp` for Arch, `dialout` for Ubuntu).



To see the device's ID, run `lsusb`:

```
1 ...
2 Bus 003 Device 018: ID 10c4:ea60 Silicon Labs CP210x UART Bridge
3 Bus 003 Device 022: ID 303a:1001 Espressif USB JTAG/serial debug unit
4 ...
```

Therefore, the vendor ID for the JTAG is 303a, and the product ID is 1001, and for the UART 10c4 and ea60.

Create a new `/etc/udev/rules.d/99-Espressif.rules` file (with `sudo!`):

- For Ubuntu/Debian/Fedora:

```
1 : Set default permissions when mounting Espressif USB JTAG/serial debug unit and UART
2 SUBSYSTEM=="usb", ENV{DEVTYPE}=="usb_device", ATTRS{idVendor}=="303a", ATTRS{idProduct}
  == "1001", GROUP="plugdev"
3 SUBSYSTEM=="tty", ATTRS{idVendor}=="10c4", ATTRS{idProduct}=="ea60", GROUP="dialout",
  MODE="0660"
```

- For Arch Linux:

```
1 : Set default permissions when mounting Espressif USB JTAG/serial debug unit
2 SUBSYSTEM=="usb", ENV{DEVTYPE}=="usb_device", ATTRS{idVendor}=="303a", ATTRS{idProduct}
  == "1001", GROUP="uucp"
```

For more information, see the JTAG documentation.

Executing the SBC gateway



Recommendations for a correct SBC setup:

- Use the recommended power supply for your SBC
- Use a good Ethernet Cable
- Use a Class 10 MicroSD card from a recognizable brand from Amazon or another reliable retailer

1. Install the OS following the SBC manufacturer's instructions
2. Create the **default folder** where your CREATOR projects will be saved, e.g. ~/creator
3. Ensure you provide the **correct rights** to the directory

```
1 sudo chown $USER:$USER ~/creator
2 sudo chmod u+rwX ~/creator
```

4. **Connect the SBC to the Internet** via Ethernet or Wi-Fi if possible. >



> Depending on the SBC's configuration, its IP may change from time to time. Check its private IP with `ip a` before each use. > An example IP would be 10.117.129.219.

5. Check the SSH service status:

```
1 systemctl status ssh
```

6. Check your username with `whoami`. Typically, it's `ubuntu`.
7. Connect to the SBC from your computer via SSH:

```
1 ssh <user>@<IP>
```



Every time an SSH connection is made, the system will ask for a password. This can be overridden by copying your computer's SSH keys to the SBC.

1. Create a new SSH key in your computer:

```
1 ssh-keygen -t rsa -b 4096
```

2. Copy the key to the SBC:

```
1 ssh-copy-id <user>@<IP>
```

8. Download and unzip the SBC gateway in the SBC
9. Set up the gateway (inside the gateway folder):

10. Create a new Python virtual environment:

```
1 python3 -m venv .venv source .venv/bin/activate
2
```

11. Install the dependencies:

```
1 pip3 install -r requirements.txt
2
```



Currently, there is a small issue in GDBGUI that needs to be patched as such:

```
sed -i "/extra_files=get_extra_files()/a\         allow_unsafe_werkzeug=True," .
    venv/lib/python3.12/site-packages/gdbgui/server/server.py
```

To validate the changes, run:

```
grep -n "allow_unsafe_werkzeug" .venv/lib/python3.12/site-packages/gdbgui/
server/server.py
```

10. Install the RISC-V Cross-Compiler on your macOS, Linux or Windows with WSL device

11. Execute the gateway:

```
1 python3 gateway.py
```

User Interface

The Target Flash menu can be accessed from *Tools* → *Flash* in the simulator view.

First, select your **device type** (ESP32 or SBC) and **target board**.

Then, provide the **target information**:

- ESP32
 - **Target port:** Port of the device's UART connection. The default values are:
 - * **Linux:** /dev/ttyUSB0
 - * **macOS:** /dev/cu.usbserial-10
 - * **Windows:** rfc2217://host.docker.internal:4000?ign_set_control
- SBC
 - **Target user:** User and IP address of the SBC (<user>@<ip>)
 - **Target location:** Location of the project folder (e.g. ~/creator)

Finally, provide the **flash URL**, the URL address of the gateway. By default, <https://localhost:8080>.

Buttons

- **Flash:** Builds and flashes CREATOR's program into your development board.

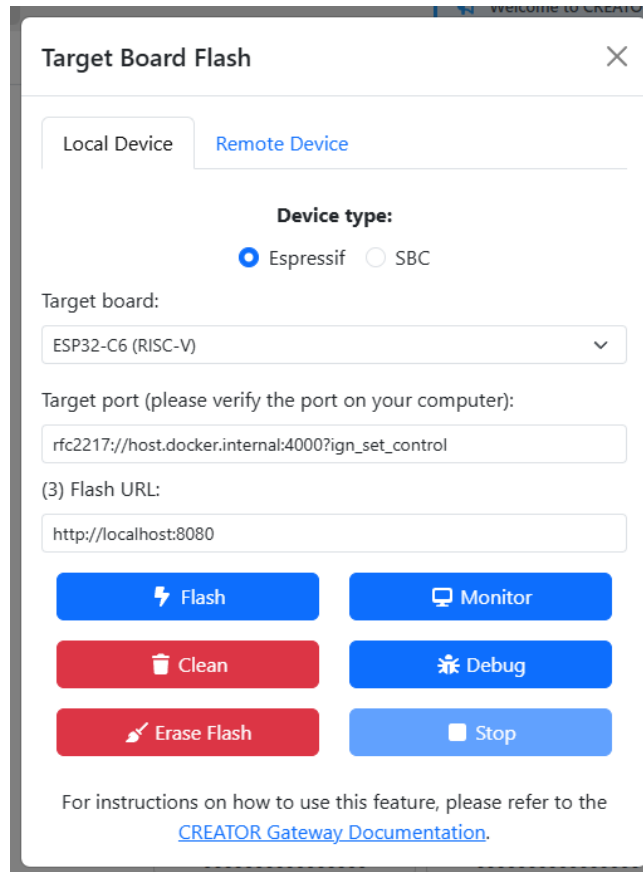


Figure 30: Target Board Flash dialog-box.

- **Monitor:** Executes development board’s flashed program. It can be stopped by using the “Stop” button or the keyboard shortcuts **Ctrl +]** or **Ctrl + t + x**.
- **Debug:** If it’s setup correctly, it will open another tab with an instance of GDBGUI ready to execute programs step-by-step.
- **Clean:** Erases gateway’s copy of the program.
- **Erase-flash:** Erases the device’s program.

Execution Control

The execution control panel allows you to run, step through, and reset your assembly programs. It provides essential controls for managing program execution within the simulator.

Execution Controls

- **Run:** Starts or resumes program execution until a breakpoint is hit or the program ends.
- **Step:** Executes the next instruction.
- **Reset:** Stops execution and resets the program state to the beginning.
- **Pause:** Temporarily halts execution, allowing you to inspect the current state.

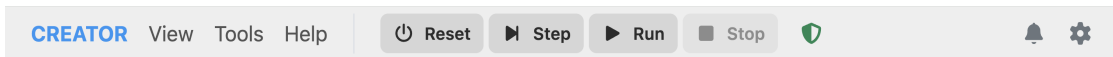


Figure 31: Execution control buttons in the simulator panel.

Breakpoints

CREATOR supports breakpoints to help with debugging. To set a breakpoint, click on any instruction in the instruction list. A red dot will appear next to the instruction, indicating an active breakpoint. When the program execution reaches a breakpoint, it will pause, allowing you to inspect registers, memory, and other state information.

Address	User Instruction	Loaded Instructions
0x0	la a0, byte	auipc a0, 512
0x4		addi a0, a0, 0
0x8	lb a0, 0(a0)	lb a0, 0(a0)
0xC	li a7, 1	addi a7, x0, 1
0x10	ecall	ecall
0x14	la a0, half	auipc a0, 512
0x18		addi a0, a0, -18
0x1C	lh a0, 0(a0)	lh a0, 0(a0)
0x20	li a7, 1	addi a7, x0, 1
0x24	ecall	ecall
0x28	li a7, 10	addi a7, x0, 10

Control registers		
PC 00000010		
Integer registers		
zero 00000000	ra 0FFFFFF0	sp 0FFFFFFC
gp 00000000	tp 00000000	t0 00000000
t1 00000000	t2 00000000	fp s0 00000000
s1 00000000	a0 0000000C	a1 00000000
a2 00000000	a3 00000000	a4 00000000
a5	a6	a7

Figure 32: Execution paused at a breakpoint.

Execution Modes

- **User Mode:** Standard execution mode with full access to user-level instructions.
- **Kernel Mode:** Elevated execution mode for system-level instructions (if supported by the architecture).

For more information, see "Privileged Instructions."

Interrupt Handling

Some architectures support interrupts. In such cases, CREATOR reacts according to the architecture's interrupt handling mechanisms. RISC-V and Z80 have their own interrupt models that are simulated accordingly.

CREATOR has two interrupt handlers: the default “CREATOR” handler, and a custom architecture-defined one. The CREATOR handler is the simplest of the two, it only handles architecture-defined system calls (see CREATOR handler), and treats all other interrupts as errors. On the other hand, the custom handler allows full control over interrupts, which requires writing a custom interrupt handler in the program.

You can modify the currently used handler in the configuration.

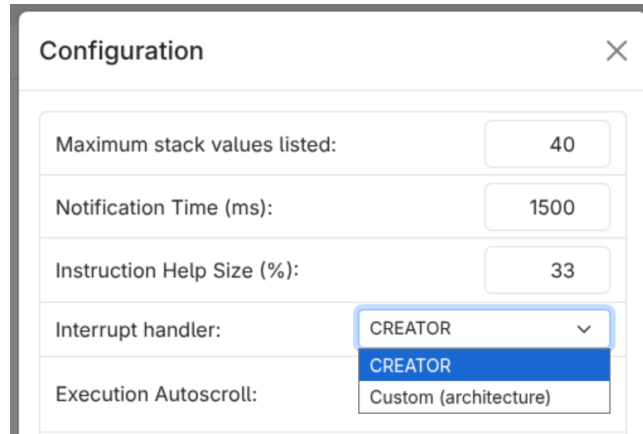


Figure 33: Modifying the interrupt handler.

For more information, see [Interrupt Support](#).

Assemblers

CREATOR has support for a modular assembler system, allowing users to choose from multiple assemblers for different architectures. This chapter provides an overview of the available assemblers, their features, and how to use them within CREATOR.

CREATOR Assembler

The default assembler built into CREATOR. This assembler is designed to work seamlessly with the defined architectures. It is currently used for RISC-V, and MIPS. Any custom architectures defined by users will, by default, also use this assembler.

Limitations

Architectures with complex instruction sets may not be fully supported. One example is the Z80 architecture, which requires a more specialized assembler due to having multiple opcodes for the same instruction based on context. Instruction sets with multiple optional fields are not supported.

RASM

RASM is a Free and open-source Z80 assembler. When choosing the Z80 architecture in CREATOR, RASM is used as the default assembler.

Choosing an Assembler

By default, the assembler is chosen based on the architecture selected. From a user perspective, there is no need to choose. The appropriate assembler will always be used automatically.

Developers creating custom architectures can specify which assembler to use in the architecture definition file.

CREATOR Arduino module (CREATino)

CREATino allows the user to add custom Arduino libraries to their programs.



This library only works with the ESP32 gateway and the supported ESP32 boards. You must set up the gateway before using this module.

Using CREATino library functions

In the Editor view, go to *Library* → *Load Arduino Library*. The available functions will be displayed on the right.



Except the `printf` function (which is exclusive for Espressif Arduino devices) all the functions displayed can be found in Arduino's documentation and in *Help* → *Creatino Help*.

Creating your first program

As in the original Arduino sketches, CREATino programs must have a structure composed by a “setup” and a “loop” function. CREATOR provides an example template in *Help* → *Examples* → *Example 1: Template for new examples*.



Before executing your program in the device, make sure to select the *Arduino Support* checkbox to enable CREATino.


```

1 setup:
2   # pinMode(30, OUTPUT);
3   li a0, 30
4   li a1, 0x03
5   addi sp, sp, -4
6   sw ra, 0(sp)
7   jal ra, pinMode
8   lw ra, 0(sp)
9   addi sp, sp, 4
10  jr ra

```

Step 2: Loop The LED has been set up; now it is we can try to make it turn on and off, creating a blinking effect. For this, we'll use the `digitalWrite` function.

This function needs the number of the pin used (pin 30) and the state to write (in this case `0x1` or HIGH to turn on the light and `0x0` to turn it off)

We will also use a delay function to generate a delay, in milliseconds, between changes of state of the LED. For this example, we'll store the length of the delay in memory.

The result is:

```

1 .data
2   time:
3     .word 1000
4
5 .text
6 loop:
7   # digitalWrite(LED_BUILTIN, HIGH);
8   li a0,30
9   li a1, 0x1
10  addi sp, sp, -4
11  sw ra, 0(sp)
12  jal ra, digitalWrite
13  lw ra, 0(sp)
14  addi sp, sp, 4
15
16  # delay(time);
17  la a0, time
18  lw a0, 0(a0)
19  addi sp, sp, -4
20  sw ra, 0(sp)
21  jal ra, delay
22  lw ra, 0(sp)

```

```

23  addi sp, sp, 4
24
25  # turn off
26
27  # digitalWrite(LED_BUILTIN, LOW);
28  li a0,30
29  li a1, 0x0
30  addi sp, sp, -4
31  sw ra, 0(sp)
32  jal ra, digitalWrite
33  lw ra, 0(sp)
34  addi sp, sp, 4
35
36  # delay(time);
37  la a0, time
38  lw a0, 0(a0)
39  addi sp, sp, -4
40  sw ra, 0(sp)
41  jal ra, delay
42  lw ra, 0(sp)
43  addi sp, sp, 4
44  j loop

```

Now the LED will start blinking.

Example 2: Button + LED

In this example we'll turn an LED on when the button is pressed.

Components:

- * ESP32-C3-DevKitC-02 board
- * Button (in GPIO 6)
- * LED (in GPIO 4)

There are two ways to do this: synchronously, using an infinite loop, and asynchronously, using interrupts.

Using an infinite loop

Step 1: Setup First we'll establish the LED as an output and the button as input. As shown in Use example 1, you need to configure the pin mode with `pinMode` before using the pins:

```

1 .data
2   buttonPin: .word 6
3   ledpin:    .word 4
4
5 .text
6
7 setup:
8   # pinMode(buttonPin, INPUT_PULLUP);
9   la a0, buttonPin
10  lw a0, 0(a0)
11  li a1, 0x05 # INPUT_PULLUP
12  addi sp, sp, -4
13  sw ra, 0(sp)
14  jal ra, pinMode
15  lw ra, 0(sp)
16  addi sp, sp, 4
17
18  # pinMode(ledpin, OUTPUT);
19  la a0, ledpin
20  lw a0, 0(a0)
21  li a1, 0x03 # OUTPUT
22  addi sp, sp, -4
23  sw ra, 0(sp)
24  jal ra, pinMode
25  lw ra, 0(sp)
26  addi sp, sp, 4
27
28  jr ra

```

Step 2: Reading the button Once set up, we start the infinite loop by reading the button state using `digitalRead`, to which we only need to pass the button's pin (in this case, pin 6).

In our case, if it detects that the button is pressed, the `button_pressed` function will be called. Otherwise, the LED will remain off. A small `delay` is added to avoid overloading the system:

```

1 .data
2   time: .word 100
3
4 .text
5 loop:
6   la a0, buttonPin
7   lw a0, 0(a0)
8   addi sp, sp, -4

```

```

9  sw ra, 0(sp)
10 jal ra, digitalRead
11 lw ra, 0(sp)
12 addi sp, sp, 4
13
14 mv t0, a0
15
16 li t1, 0 # LOW
17
18 beq t0, t1, button_pressed
19
20 la a0, ledpin
21 lw a0, 0(a0)
22 li a1, 0x0
23 jal ra, digitalWrite
24
25 la a0, time
26 lw a0, 0(a0)
27 addi sp, sp, -4
28 sw ra, 0(sp)
29 jal ra, delay
30 lw ra, 0(sp)
31 addi sp, sp, 4
32
33 j loop

```

Step 3: Turning the LED on As shown in Example 1, we will turn on the LED when button is pressed:

```

1 button_pressed:
2   la a0, ledpin
3   lw a0, 0(a0)
4   li a1, 0x1
5   addi sp, sp, -4
6   sw ra, 0(sp)
7   jal ra, digitalWrite
8   lw ra, 0(sp)
9   addi sp, sp, 4
10
11  la a0, time
12  lw a0, 0(a0)
13  addi sp, sp, -4

```

```

14  sw ra, 0(sp)
15  jal ra, delay
16  lw ra, 0(sp)
17  addi sp, 4
18
19  jr ra

```

Using interrupts

Another way to achieve this project is by using GPIO interrupts, which are much more immediate but more complex to program.

In this case, we will use the `attachInterrupt` and `digitalPinToInterrupt` Arduino functions to obtain the interrupt number that can be assigned to the interrupt service routine for that pin.

Step 1: Setup As shown in Example 1, you need to configure the pin mode with `pinMode` before using the pins. Then we connect the button pin to an interrupt routine or ISR (which we will call `blink`) that runs automatically when the button is pressed. For this we will use `attachInterrupt` function.

The `attachInterrupt` function takes the following parameters: - The interrupt position corresponding to the pin for which we want to detect the interrupt (we use `digitalPinToInterrupt(pin)`) - The memory address where the interrupt service routine is located (in this case, we call it `blink`) - The interrupt mode, that can be one of the following:

Mode	Value	Usage
DISABLED	0x00	Interrupt disabled
RISING	0x01	Interrupt triggered on the rising edge (when the pin changes from LOW to HIGH)
FALLING	0x02	Interrupt triggered on the falling edge (when the pin changes from HIGH to LOW)
CHANGE	0x03	Interrupt triggered on any change of the pin state (both LOW→HIGH and HIGH→LOW)
ONLOW	0x04	Interrupt triggered while the pin remains LOW
ONHIGH	0x05	Interrupt triggered while the pin remains HIGH
ONLOW_WE	0x06	Same as ONLOW, but with write enable — allows modifications or writing to related registers while the pin is LOW
ONHIGH_WE	0x07	Same as ONHIGH, but with write enable

In this case, as we want the interruption when the button is pressed, we choose the `ON_LOW` mode.

This is how the `setup` function will look:

```

1  .data
2  ledPin:      .byte 4

```

```
3 interruptpin: .byte 6
4 state:      .byte 0 #LOW
5 on_low:    .byte 0x04
6
7 .text
8 setup:
9 # pinMode(ledPin, OUTPUT);
10 la t1, ledPin
11 lb a0, 0(t1)
12 li a1, 0x03 # OUTPUT
13 addi sp, sp, -4
14 sw ra,0(sp)
15 jal ra, pinMode
16 lw ra,0(sp)
17 addi sp, sp, 4
18
19 # pinMode(ledPin, INPUT_PULLUP);
20 la t1, interruptpin
21 lb a0, 0(t1)
22 li a1, 0x05 # INPUT_PULLUP
23 addi sp, sp, -4
24 sw ra,0(sp)
25 jal ra, pinMode
26 lw ra,0(sp)
27 addi sp, sp, 4
28
29 # digitalPinToInterrupt(interruptpin);
30 la t1, interruptpin
31 lb a0, 0(t1)
32 addi sp, sp, -4
33 sw ra,0(sp)
34 jal ra, digitalPinToInterrupt
35 lw ra,0(sp)
36 addi sp, sp, 4
37
38
39 # attachInterrupt(digitalPinToInterrupt(interruptPin), blink, ON_LOW);
40 la a1, blink
41 la t1, on_low
42 lb a2, 0(t1)
43 addi sp, sp, -4
44 sw ra,0(sp)
```

```

45 jal ra, attachInterrupt
46 lw ra,0(sp)
47 addi sp, sp, 4
48
49 jr ra

```

Step 2: ISR definition. We want to change the LED state when an interrupt is detected (the button's state changes). For that, we'll modify a variable stored in memory that indicates the LED's state, as follows:

```

1 blink :
2   addi sp, sp, -8
3   sw ra, 4(sp)
4   sw t0, 0(sp)
5
6   la t0, state
7   lb a0, 0(t0)
8   xori a0, a0, 1 # 0->1, 1->0
9   sb a0, 0(t0)
10  lw t0, 0(sp)
11  lw ra, 4(sp)
12  addi sp, sp, 8
13  jr ra

```

Step 3: Loop The LED will be turned off until the button is pressed, as shown in the following code:

```

1 loop :
2
3   # digitalWrite(ledPin, state);
4   la t1, ledPin
5   lb a0, 0(t1)
6   li a1,0
7   addi sp, sp, -4
8   sw ra,0(sp)
9   jal ra, digitalWrite
10  lw ra,0(sp)
11  addi sp, sp, 4
12
13  # delay(100)
14  li a0, 100
15  addi sp, sp, -4

```

```
16  sw ra,0(sp)
17  jal ra, delay
18  lw ra,0(sp)
19  addi sp, sp, 4
20  j loop
21
22  setup:
23
24  # pinMode(ledPin, OUTPUT);
25  la t1, ledPin
26  lb a0, 0(t1)
27  li a1, 0x03 #OUTPUT
28  addi sp, sp, -4
29  sw ra,0(sp)
30  jal ra, pinMode
31  lw ra,0(sp)
32  addi sp, sp, 4
33
34  # pinMode(ledPin, INPUT_PULLUP);
35  la t1, interruptpin
36  lb a0, 0(t1)
37  li a1, 0x05 # INPUT_PULLUP
38  addi sp, sp, -4
39  sw ra,0(sp)
40  jal ra, pinMode
41  lw ra,0(sp)
42  addi sp, sp, 4
43
44  # digitalPinToInterrupt(interruptpin);
45  la t1, interruptpin
46  lb a0, 0(t1)
47  addi sp, sp, -4
48  sw ra,0(sp)
49  jal ra, digitalPinToInterrupt
50  lw ra,0(sp)
51  addi sp, sp, 4
52
53  # attachInterrupt(digitalPinToInterrupt(interruptPin), blink, CHANGE);
54  la a1, blink
55  la t1, change
56  lb a2, 0(t1)
57  addi sp, sp, -4
```

```

58  sw ra,0(sp)
59  jal ra, attachInterrupt
60  lw ra,0(sp)
61  addi sp, sp, 4
62
63  jr ra

```

Example 3: Text input/output using serial output

For this use case, we are going to make a little use of basic functions from the Arduino Serial library. For more information, here is the official documentation (not all functions are available in this library, as they are not the most suitable for the environment in which we are working).



By definition, serial input functions are very fast (they do not wait for you to press Enter) and do not display a callback of what has been written. The purpose of this library is to familiarize yourself with these functions; therefore, **it is the student's responsibility to monitor each step** of what is being done.

Just as we previously used the `ecall` instruction to print messages in assembly CREATOR programs, here we will use the `serial_printf` function, which is part of Espressif's Arduino component.

Unlike higher-level functions like `Serial.print` and `Serial.println`, `serial_printf` requires explicit format specifiers to indicate the data types being printed; otherwise, the output is interpreted as a string.

On the other hand, we will use the `serial_readBytes` function to see how text input works. There is the `serial_read` variant (which only takes 1 character), `serial_readBytesUntil` (which stops storing characters when it finds the specified character), and those that parse, such as `serial_parseInt` (which only takes numbers).

Components:

- ESP32-C3-DevKitC-02 board

Step 1: Data Save messages to print in memory. For this use case we are going to declare in data section:

- The initial message to be displayed.
- The buffer allocated to store the input text.
- The message that includes a placeholder for outputting the entered text.
- An auxiliary callback used to display the entered number.

This would be reflected in the code as follows:

```

1 .data
2   space:   .zero 100 # Buffer to place the string
3   initial: .string "Introduce number of letters:\n"
4   aux:     .string "%d\nType your message\n"
5   print:   .string "Your message: %s\n"

```

Step 2: Serial Start terminal output and input. On most boards, such as Arduino and Espressif, in order to use the terminal, it needs to be initialized with a specific frequency. In this case, we will use the `serial_begin` function with a baud rate of 115200.

If a value other than the one given is entered, strange characters may be printed or nothing may be printed at all.

It is declared in the code as follows:

```

1 setup: li a0, 115200
2       addi sp, sp, -4
3       sw ra, 0(sp)
4       jal ra, serial_begin
5       lw ra, 0(sp)
6       addi sp, sp, 4
7       jr ra

```

Step 3: Loop Check if the terminal is correctly open. A good practice that can be seen in Arduino is to use `serial_available` to see if the terminal has opened correctly.

If it has a value greater than 0, it means that it is operational and ready to use.



For simplicity's sake, you will often find that this check is not performed... but using `serial_available` is a very good error control.

So, we start our loop as follows:

```

1 loop: addi sp, sp, -4
2       sw ra, 0(sp)
3       jal ra, serial_available
4       lw ra, 0(sp)
5       addi sp, sp, 4
6       beqz a0, aux_print
7       j loop

```

'aux_print' is an auxiliary function to indicate to the user that they should enter the number only once. This is purely aesthetic but can provide clarity to the user.

```

1 aux_print: # serialPrintf
2     la a0, initial
3     addi sp, sp, -4
4     sw ra, 0(sp)
5     jal ra, serial_printf
6     lw ra, 0(sp)
7     addi sp, 4
8     j read_num

```

‘read_num’: reads a number from terminal

In this case, we use the ‘serial_parseInt’ function to get a number per terminal.



Why don't we use "serial_read"? Because "serial_read", although it returns a number, interprets the input in ASCII code.

If we enter the number '4' via the terminal, the values change:

- - In 'serial_read': 52
- - In 'serial_parseInt': 4

Since 'serial_read' is very fast, we will not move on to the next step if there is no number greater than 0 collected in a0, leaving the following code snippet:

```

1 read_num: addi sp, sp, -4
2     sw ra, 0(sp)
3     jal ra, serial_parseInt
4     lw ra, 0(sp)
5     addi sp, sp, 4
6     mv t0, a0
7     bnez t0, print_int
8     j read_num

```

A small auxiliary function called `print_int` was created to view the callback of the value specified as length, as follows.

```

1 print_int:
2     la a0, aux
3     mv a1, t0
4     addi sp, sp, -4
5     sw ra, 0(sp)
6     jal ra, serial_printf
7     lw ra, 0(sp)
8     addi sp, 4
9     j read_function

```

The `read_function` reads the text of the requested length. Once we have the length of our string, we collect the text we want to add with `serial_readBytes`, which is blocking until the requested length of characters has been reached.

We would end up with an implementation like this:

```

1 read_function:
2     la a0, space
3     mv a1, t0 # number of letters it will have
4     addi sp, sp, -4
5     sw ra, 0(sp)
6     jal ra, serial_readBytes
7     lw ra, 0(sp)
8     addi sp, sp, 4
9     bne t0, a0, read_function
10    la a0, print
11    la a1, space
12    addi sp, sp, -4
13    sw ra, 0(sp)
14    jal ra, serial_printf
15    lw ra, 0(sp)
16    addi sp, 4
17    jr ra

```

And this is the result!

Example 4: Daytime running lights with `analogRead`.

This time, we are going to make a small LED that lights up when it detects low light, using an LDR.



The sensitivity values of the sensor may vary depending on the location of the student and their device. We recommend having a flashlight or something that gives off light handy and using the debugger or prints.

Components:

- ESP32-C3-DevKitC-02 board
- LDR or photoresistor (in GPIO 2)
- LED (in GPIO 4)
- 10k Ω resistor

To find resistors with the correct value, look at the color code on their bands. You can either look at the color guide, use this calculator, or simply look for a resistor that matches the one in the photo.

Step 1: Setup Initialize LDR, pin, and serial output. To use the sensor, we must initialize it with `pinMode` to the value of `INPUT` (0x01) as we saw in Figure 2.1. The setup code would look like this:

```

1 .data
2     lightSensorPin: .word 2
3     ledPin: .word 4
4     time: .word 100
5     aux_msg: .string "LDR value: %d\n"
6
7 .text
8 setup:
9     # Serial
10    li a0,115200
11    addi sp, sp, -4
12    sw ra, 0(sp)
13    jal ra, serial_begin
14    lw ra, 0(sp)
15    addi sp, sp,4
16
17    # PinMode LED
18    la t1, ledPin
19    lw a0, 0(t1)
20    li a1, 0x03 # OUTPUT
21    addi sp, sp, -4
22    sw ra,0(sp)
23    jal ra, pinMode #pinMode(ledPin, OUTPUT);
24    lw ra,0(sp)
25    addi sp, sp, 4
26
27    # Light sensor pin
28    la t1, lightSensorPin
29    lw a0, 0(t1)
30    li a1, 0x01
31    addi sp, sp, -4
32    sw ra,0(sp)
33    jal ra, pinMode# pinMode(lightSensorPin, INPUT);
34    lw ra,0(sp)
35    addi sp, sp, 4
36
37    jr ra

```

Step 2: Loop Analog sensor reading Once everything is up and running, we read the light level in the room using `analogRead`.

In this tutorial, after a few tests, we found that the values reached were **between 1100 and 1400**. The darker it is, the higher the resistance value will be. **Therefore, a threshold of 1200 is set.**

- If the sensor reaches a value higher than 1200, the LED will turn on (`lightUp`).
- If, on the other hand, it does not reach that value, the LED remains off (`turnDown`).

In both cases, we add a small `delay` so that the readings are not so fast.

We end with this code:

```

1  # delay
2  la a0, time
3  lw a0, 0(a0)
4  addi sp, sp, -4
5  sw ra, 0(sp)
6  jal ra, delay
7  lw ra, 0(sp)
8  addi sp, sp, 4
9
10 loop: # read LDR
11  addi sp, sp, -4
12  sw ra, 0(sp)
13  jal ra, analogRead
14  # analogRead(lightSensorPin);
15  lw ra, 0(sp)
16  addi sp, sp, 4
17
18  # Print value
19  mv t1, a0
20  mv a1, a0
21  la a0, aux_msg
22  addi sp, sp, -4
23  sw ra, 0(sp)
24  jal ra, serial_printf
25  lw ra, 0(sp)
26  addi sp, sp, 4
27
28  # turn up led
29  li t0, 1200 #Minimun value
30  bgt t1, t0, lightUp
31  blt t1, t0, turnDown

```

32
33`j loop`

And this is the result:

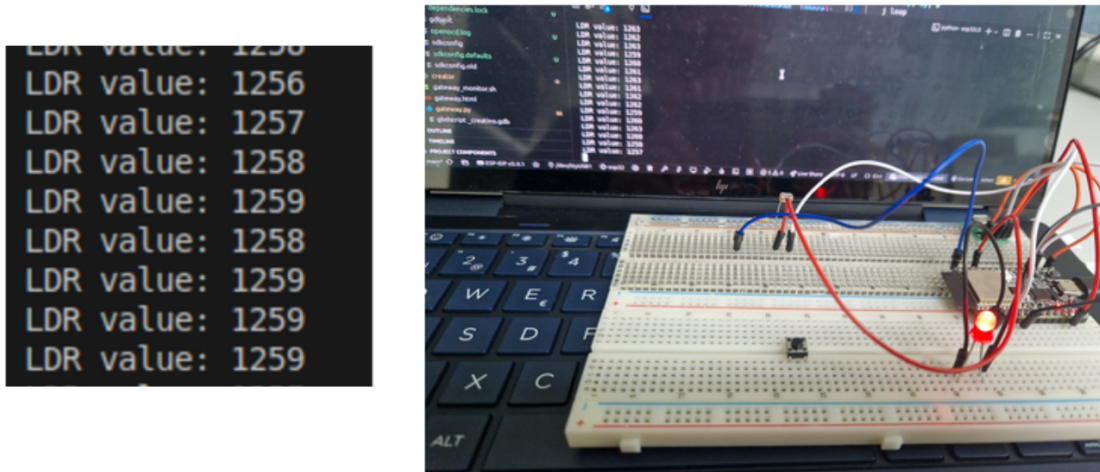


Figure 34: Arduino example 4.

Example 5: [Advanced] Piano

This case is a little more complex than the rest, but very creative. It is recommended to have a breadboard with plenty of space.

Each musical note is a frequency that blows air into the buzzer membrane. Consult [this page](<https://www.tibotinspirationlab.com/reto/musica-con-arduino/>) to learn how to calculate the other possible notes according to the desired tempo.

In this case, we are going to do it with interruptions. This example may cause a little more lag because there are continuous memory accesses and the “tone” function launches tasks.

Polling could be used.

Components:

- ESP32-C3-DevKitC-02 board
- 4 buttons
- A passive buzzer

Step 1: Data Declaration of pins and values of musical notes. We indicate in the data the pins we are going to use (avoiding “dangerous” pins such as ‘GPIO8’ and ‘GPIO1’) and the frequency values of the musical notes.

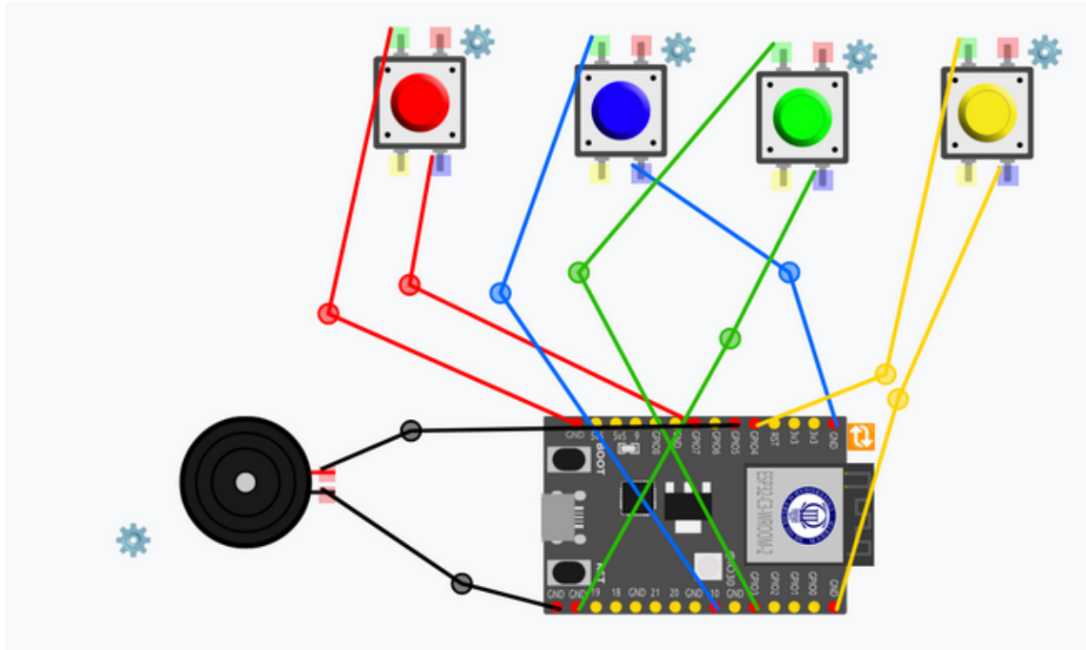


Figure 35: Arduino setup.

Care must be taken with the position of these values, as we are going to use these memory positions as arrays.

In this example, we have positioned them as follows:

```

1 .data
2 # GPIO
3 buzzerPin: .word 5
4 button_C4: .word 7
5 button_D4: .word 10
6 button_E4: .word 3
7 button_G4: .word 4
8
9 # Notes
10 note_C4: .word 262
11 note_D4: .word 294
12 note_E4: .word 330
13 note_G4: .word 392
14
15 #aux
16 button_count: .word 4
17 time_delay: .word 10
18 anyPressed: .word -1
19 .align 4

```

```

30 button_handlers:
31     .word  handleButton0
32     .word  handleButton1
33     .word  handleButton2
34     .word  handleButton3

```

Another way to position them is like this:

```

1  .data
2  # GPIO
3  buzzerPin: .word 5
4  buttons:   .word 7,10,3,4
5
6  # Notes
7  notes:    .word 262,294,330,392
8
9  # aux
10 button_count: .word 4
11 anyPressed:  .byte -1
12
13 .align 4
14 button_handlers: .word  handleButton 0
15                 .word  handleButton 1
16                 .word  handleButton 2
17                 .word  handleButton 3

```

Step 2: Setup Configure all pins In this case, we are going to complicate things a little, as there are a lot of pins to configure. First, we will configure pin 5 of the buzzer, which, unlike the buttons, will use an OUTPUT mode (since it emits a sound to the outside).

```

1  setup:
2     # buzzer
3     la a0, buzzerPin
4     lw a0, 0(a0)
5     li a1, 0x03 #OUTPUT
6     addi sp, sp, -4
7     sw ra, 0(sp)
8     jal ra, pinMode
9     lw ra, 0(sp)
10    addi sp, sp, 4

```

Then, to configure the rest of the buttons, we created a loop that goes through all the selected buttons.

First, in setup, after initializing the buzzer, we initialize the variables in our loop:

```

1   la  s0, button_C4
2   # Button list
3   li  s1, 0
4
5   # Position in the list
6   la  t3, button_count
7   lw  s2, 0(t3)
8
9   # List length

```

Next, we move on to the `loop_buttons` function, where we will:

- Check if we have already gone through the entire list

```

1   loop_buttons: bge s1, s2, end_loop_buttons # loop until all the
                # buttons are positioned

```

- If this is not the case, we scroll through the data to find the pin number we want.

```

1   # Take position of the button
2   slli s3, s1, 2
3   add  t1, s0, s3 # shift
4   lw  s4, 0(t1) # Button value mv a0, s4

```

- Once the position has been obtained, we configure the button with `INPUT_PULLUP` mode, as they are buttons.

```

1   li  a1, 0x05 # INPUT_PULLUP
2   addi sp, sp, -4
3   sw  ra, 0(sp)
4   jal ra, pinMode
5   lw  ra, 0(sp)
6   addi sp, sp, 4

```

- As we indicated in the statement, we are going to use interrupts, so we have to assign them now knowing which button we are on (that is, we take advantage of the fact that the order of `button_handlers` is the same as the order followed by the button array). For more information on how to assign interrupts, see example 2. We will indicate what the ISRs are like in the next point:

```

1   # Attach Interrupts
2   # Transform digitalPin into interrupt
3   mv  a0, s4
4   addi sp, sp, -4

```

```

6  sw ra,0(sp)
7  jal ra, digitalPinToInterrupt #
   digitalPinToInterrupt(interruptpin);
8
9  lw ra,0(sp)
10 addi sp, sp, 4 # Search the correct pointer la t0, button_handlers
11 add t1, t0, s3
12 lw a1, 0(t1) # Let the interrupt jump when button is pressed
   (on_low)
13 li a2, 0x03
14 addi sp, sp, -4
15 sw ra,0(sp)
16 jal ra, attachInterrupt #
   attachInterrupt(digitalPinToInterrupt(buttonPin[i]),
   handler[i], ON_LOW);
17 lw ra,0(sp)
   addi sp, sp, 4

```

- We add up a position and re-enter the loop

```

1  addi s1, s1, 1 # next button
2  j loop_buttons

```

- If we have finished going through the list, we return to main by executing a `ret` (or a `jr ra`).

```

1  end_loop_buttons: ret

```

Step 3: Loop This step can be done in two ways: with polling (i.e., constantly checking the status of all buttons) or with interrupts (pressing the button triggers an interrupt). The easiest way to do this exercise is to assign an interrupt to each button and, when pressed, have each one have its own ISR. Therefore, before starting the loop, we will create each of the necessary ISRs and assign them to the buttons. Refer to case 2 using interrupts for a better understanding.

In this case, we use a “flag” change since the `tone()` function underneath launches “tasks” or “processes” underneath, which is not safe to do in an ISR.

```

# ISR handleButton0:
1  la t0, anyPressed
2  lw t1, 0(t0)
3  li t2, 0 # Assign button
4  sw t2, 0(t0)
5  jr ra
6
7
8  handleButton1:

```

```

9   la t0, anyPressed
10  lw t1, 0(t0)
11  li t2, 1 # Assign button
12  sw t2, 0(t0)
13  jr ra
14
15  handleButton2:
16  la t0, anyPressed
17  lw t1, 0(t0)
18  li t2, 2 # Assign button
19  sw t2, 0(t0)
20  jr ra
21
22  handleButton3:
23  la t0, anyPressed
24  lw t1, 0(t0)
25  li t2, 3 # Assign button
26  sw t2, 0(t0)
27  jr ra

```

Then, inside the loop, we check the status of the `anyPressed` flag and add a small `delay` so that the watchdog does not trip.

This loop checks that, if the flag is not at -1, the tone corresponding to that position sounds.

```

1  loop: la t0, anyPressed
2      lw s0, 0(t0)
3      li t1, -1
4      bne s0, t1, startTune
5      la t0, time_delay
6      lw a0, 0(t0)
7      addi sp, sp, -4
8      sw ra, 0(sp)
9      jal ra, delay # delay(200);
10     lw ra, 0(sp)
11     addi sp, sp, 4
12     j loop

```

Step 4: Start Tune Start playing the tone.

In this case, once we have the position of the button that has been pressed, we search the memory array for the corresponding note value, similar to when we searched for the button.

To prevent the tone from having an indefinite duration, we have set a timeout of 200. Once the

tone is played, it returns to the loop.

```
1 startTune:
2   # Clean value
3   la t0, anyPressed
4   li t1, -1
5   sw t1, 0(t0)
6
7   # Search value
8   la t0, note_C4
9   slli s1, s0, 2
10  add t1, s1, t0
11  lw s2, 0(t1) # Note value
12
13  # Play Tone
14  la t0, buzzerPin
15  lw a0, 0(t0)
16  mv a1, s2
17  li a2, 200
18
19  # tone(buzzerPin, notes[i], duration);
20  addi sp, sp, -4
21  sw ra, 0(sp)
22  jal ra, tone
23  lw ra, 0(sp)
24  addi sp, sp, 4
25
26  j loop
```

USER MANUAL AND USE CASES FOR THE SAIL-BASED MODEL

In this chapter, we will present the user manual for the new Sail-based simulator engine, using a simple example program, and show different use cases for the tool.

User manual

This user manual describes the different functionalities integrated into the new RISC-V simulator based on the Sail specification language.

Init page

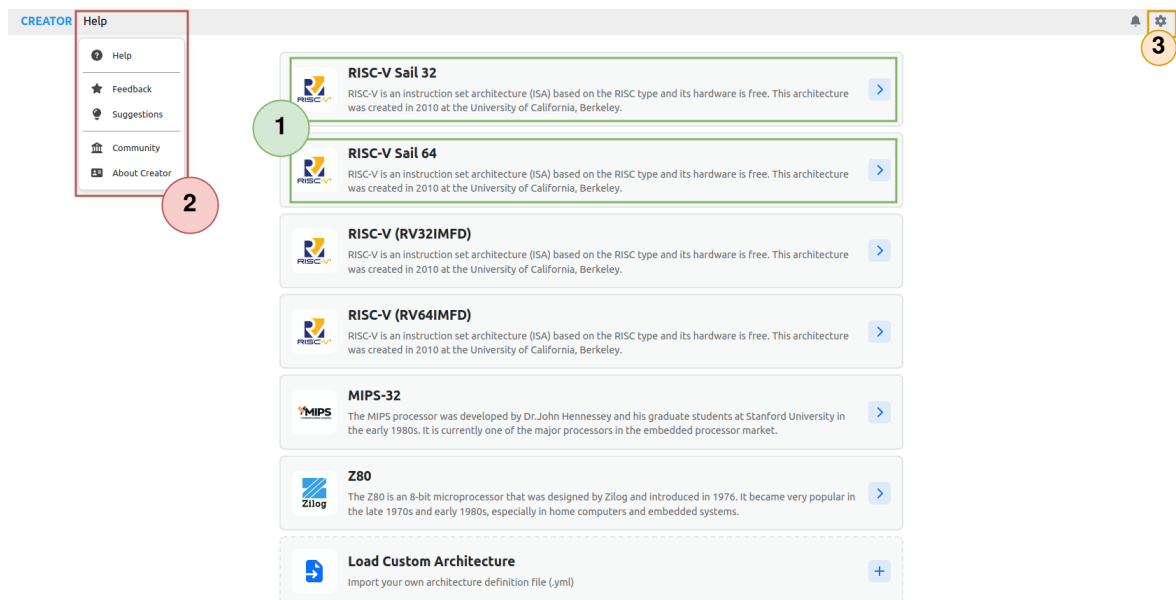


Figure 36: Simulator home page

The simulator's home page lists the available architectures for simulation, as shown in Figure 36.

First, in the central area, two variants of the RISC-V architecture are implemented with Sail. Remember that for each module, the complete set of instructions for each architecture is available. You can access the simulator directly by selecting the architecture variant to be used, as shown in the highlighted area **1**. On the other hand, we have the help menu in case any error or unwanted behavior is identified while using the tool, as shown in the highlighted area **2**. Finally, there is a configuration menu where you can edit the simulator's characteristics, as shown in the highlighted area **3**.

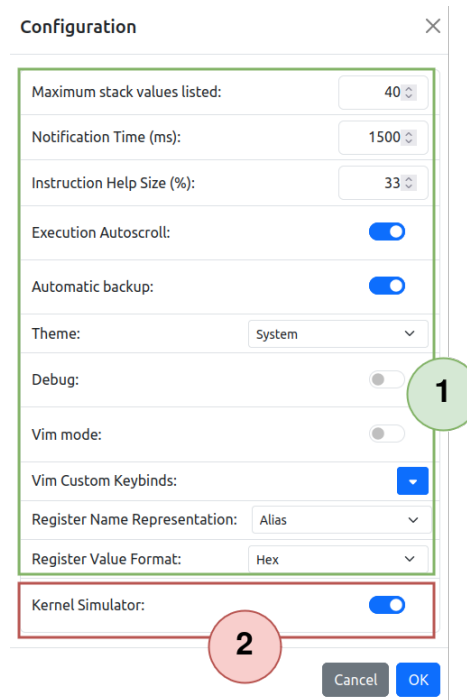


Figure 37: Módulo de configuración del simulador web

The Figure 37 corresponds to the simulator configuration menu. This menu allows the user to configure different aspects of the simulator to adapt its execution to their needs. The highlighted area **1** shows additional visual aspects of the simulator configuration, such as displaying messages during debugging, the code editor, and how records are represented, among others. The highlighted area **2** allows the user to select whether the user wants to use the kernel implementation integrated into the simulator itself or a kernel developed by the user for program execution.

Once the simulator is configured through the modules presented, it proceeds to select the architecture, as shown in the highlighted area **1** of Figure 36, and accesses the simulation module.

Simulation module

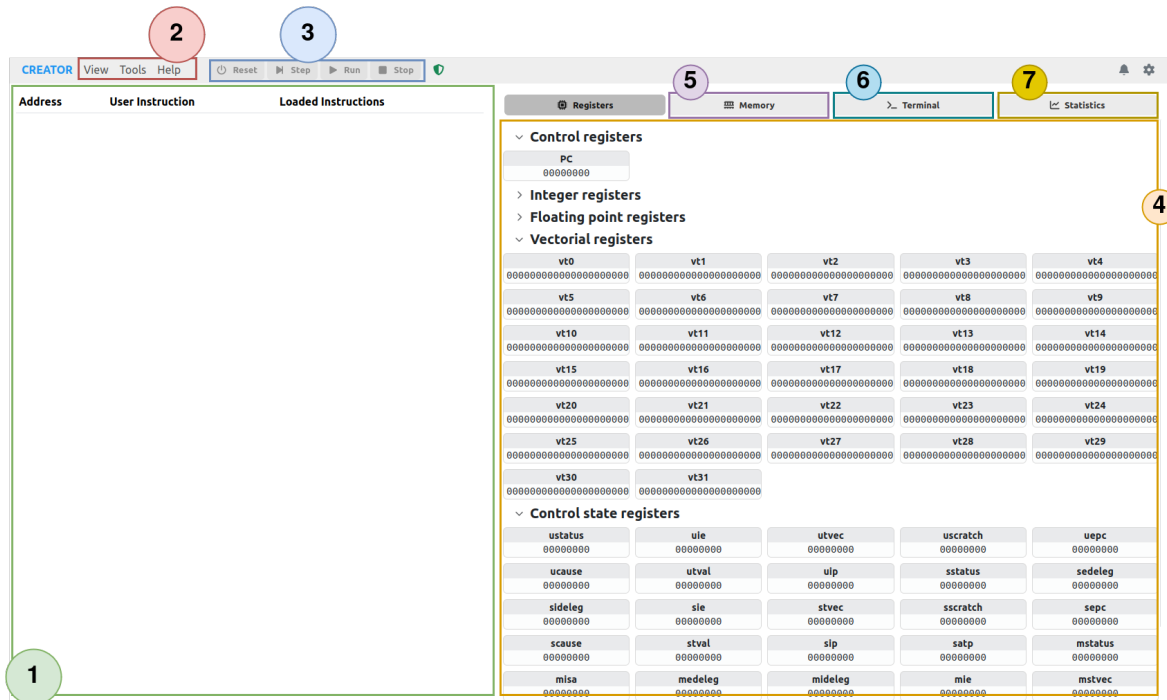


Figure 38: Módulo de simulación del simulador Web

As shown in Figure 38, different sections are identified within the simulator's execution module. Moving from left to right, the module's elements are identified.

On the left side, different areas are identified:

1. Instruction execution and debugging area: this section shows the coding and address of the compiled assembly instructions, allowing you to track the current status of the architecture. Also, the user can set a breakpoint on a specific instruction to stop execution and debug its behavior if the program was run without interruptions, not step by step.
2. Simulator navigation bar: allows you to navigate the simulator's views and elements. In the *View* section, you can navigate to the code editing module or the architecture information module; the *Tools* section allows you to load examples of the architecture, use the calculator, or use the remote service to flash on a microcontroller; and the *Help* section, as shown in Figure 36, allows you to access the simulator's help and contact module.
3. Simulator execution bar: This allows the user to execute their programs step by step, run them without interruptions, stop execution, and reset execution.

On the right side, the following areas are identified:

4. Architecture status: Displays the current state of the architecture's registers. On each register, you can see the value stored in the register and view it in different representations (hexadecimal, decimal, IEEE 754, etc.).

5. Architecture Memory View: Displays the contents of the Memory and is updated during program execution.
6. Terminal View: shows the program's input and output during execution.
7. Statistics View: shows the program's execution statistics, displaying which instruction types are executed.

In the Tools area, there is a button that opens a menu of programs to run in the simulator. Its function is to learn about programming in the simulator and understand the architecture's functionalities, as shown in Figure 39. This menu can be accessed via the Tools button in Figure 38.

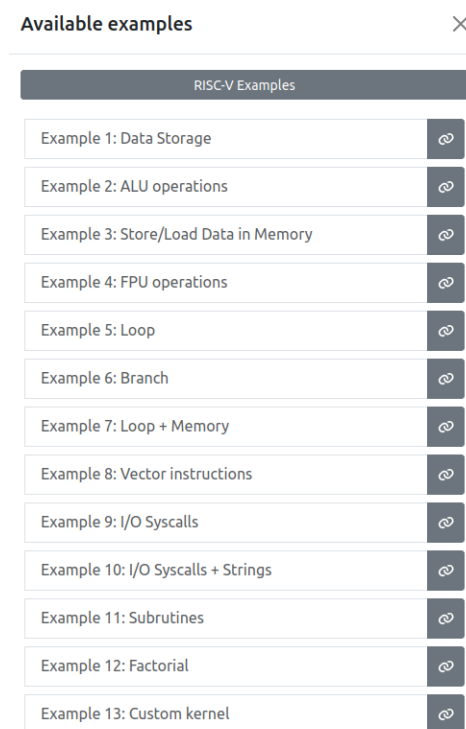


Figure 39: RISC-V program examples menu.

In the same tools area, there is a button that redirects to an IEEE 754 calculator/converter between decimal, hexadecimal, and single and double precision floating point values, in 32 and 64 bits, as shown in Figure 40. It can be accessed through the tools menu, as shown in Figure 38.



Figure 40: Calculator/converter IEEE 754 of decimal, hexadecimal, simple, and double precision values .

The architecture area shows the user the configuration set for that variant in the simulator, as shown in Figure 41. You can navigate through it to see the instructions available to the user within the simulator. As shown in the highlighted area 1, the user can view the instructions, pseudo-instructions, directives, and registers available in the architecture. Finally, in the highlighted area 2, the user is shown a summary of the configuration established in the simulator, including the word size, the name of the main function, memory alignment, parameter-passing convention, etc.

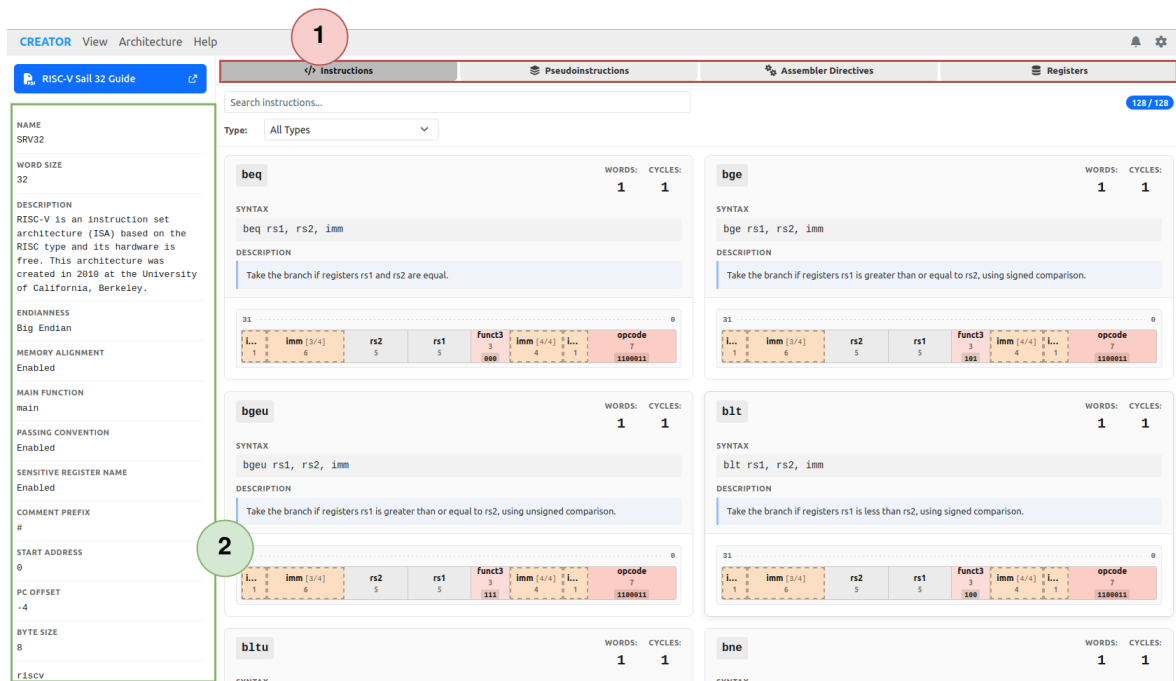


Figure 41: 32-bit RISC-V architecture configuration.

Code editor module

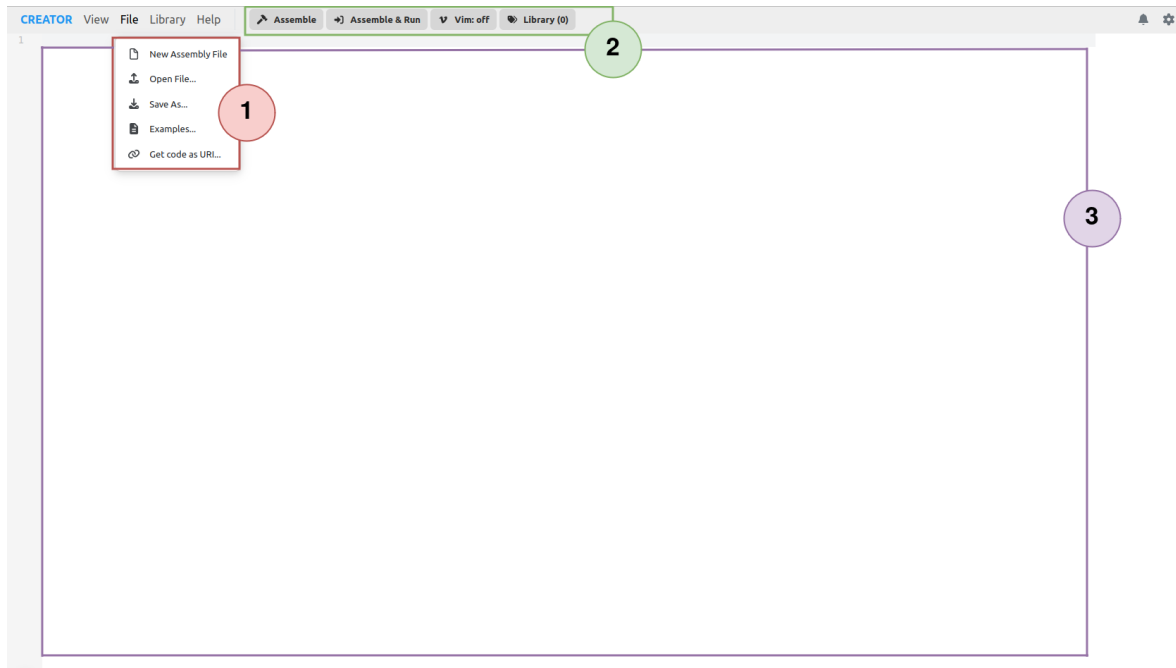


Figure 42: Program coding module.

As shown in Figure 42, different parts or modules are identified in the editor: program coding and compilation (highlighted area **2**), file creation, loading, and downloading (highlighted area **1**); and library creation, loading, and downloading (*Library* menu button).

Files can be created using the “New File” button in the highlighted area **1**. In addition, this menu can be used to load files that have been previously coded for the project, load examples such as those in Figure 39, and even download files coded in the editor (highlighted area **3**). After creating or loading files in the editor, a message will appear in the code editing view to indicate whether the operation was successful.

For libraries, there is a menu for creation and loading (*Library* menu options). Once the program with which you want to generate the library has been coded (**it is important that the program does not contain the (*main*) functionality, otherwise the library cannot be generated**), it is compiled and, once the user is notified that it has been compiled correctly, the tool is asked to generate a new library. This option downloads the created library to the user’s device. On the other hand, to load libraries, use the “Load” option in the library menu and select the libraries to be included in the editor. Once the library has been loaded correctly, a message will be displayed on the screen to notify the user.

For coding, the contents of the file will be displayed. Once the files required to generate the program or library have been encoded, proceed to compile and generate the binary to be executed by pressing the compilation button in the highlighted area **2**.

Once the program has been generated, you can download it as a library (if it does not contain the

support the user.

mode, for example); or from which execution mode it comes from at the moment the interrupt or exception occurs. Finally, the highlighted area **3** shows the start address of execution, which in this case is the kernel, not the main function.

Execution of a program with vector instructions.

For this use case, use the "Example8.s" from the examples menu. This code it is an implementation of how to load, operate, and store vectors. This example can be modified in the Editor's view to test with other vector data types, for example, floats, integers, bytes, or halves.

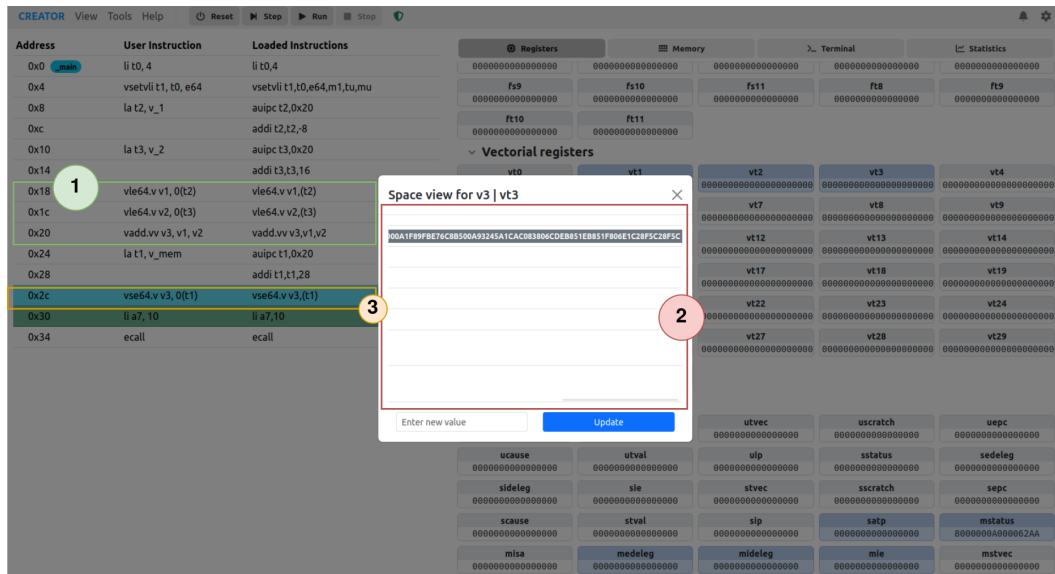


Figure 46: Program execution with vectors.

As shown in Figure 46, in the highlighted section **1**, the program execution is computed as the sum of two vectors *y*, the result of which is stored in the highlighted area **2**. The hexadecimal value shown is the result of the sum. However, the result will be stored at the memory address specified by the storage instruction in the highlighted area **3**. Once stored in memory or the execution has finished, the result value can be checked in the memory view.

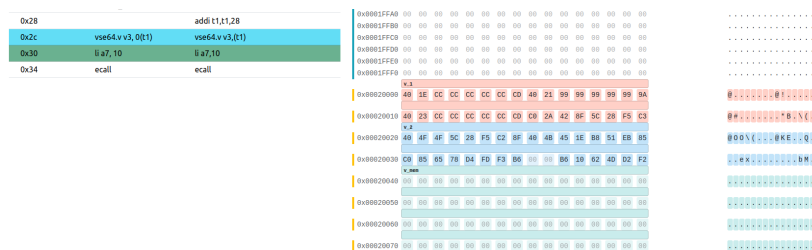


Figure 47: Result vector values stored in memory.

As shown in Figure 47, the result is successfully stored in memory in "v_mem" address assigned to store the result vector.

Execution of a program compiled with a library which was previously generated.

For this use case, two files have been used for the development.

```

1 # auxiliary program code
2 .section .data
3 .align 4
4 pi:
5     .float 3.141516
6
7 .section .text.init
8 .globl circumference_area
9
10 circumference_area:
11     la t0, pi
12     flw ft0, 0(t0)
13     fcvt.s.w ft1, a0
14     fmul.s ft2, ft1, ft1
15     fmul.s fa0, ft2, ft0
16     li a7, 2
17     ecall
18     jr ra

```

Figure 48: Auxiliary assembly program which calculate the area of a circumference.

```

1 # main program code
2 .section .data
3 .align 2
4 radio:
5     .word 8
6
7 .section .bss
8 .align 8
9 tohost: .dword 0
10
11 .section .text.init
12 .globl __main
13
14 # Complete your main function here
15 __main:
16     la t0, radio
17     lw a0, 0(t0)
18     call circumference_area
19     li a7, 10
20     ecall

```

Figure 49: Main assembly program which call the function of the library.

The listing file in Figure 48 is used to generate a library that is downloaded after compilation and then loaded into the simulator. The listing file in Figure 49 is used to call the program's main function, and within the main function, the function from the library is called.

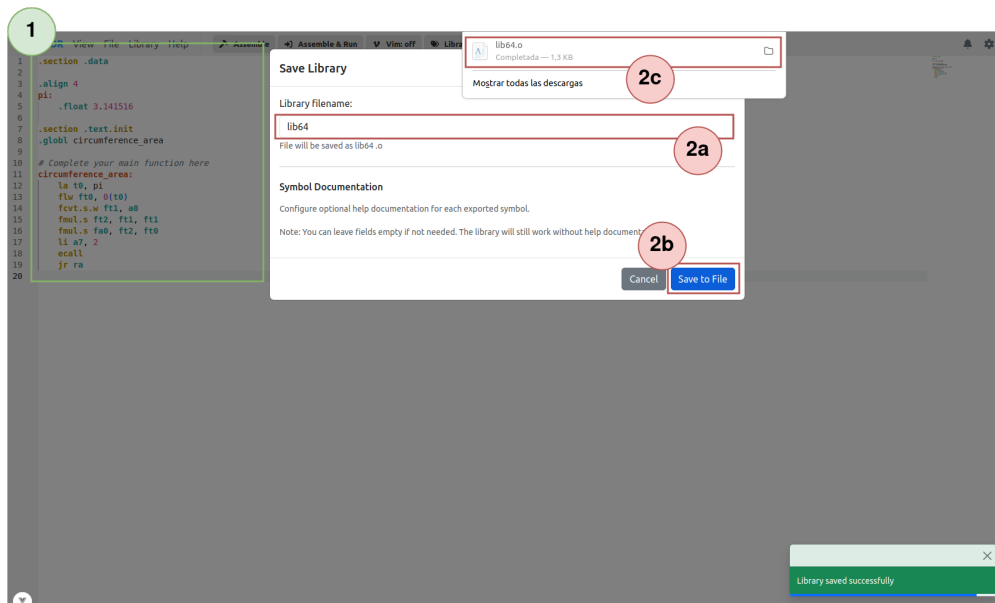


Figure 50: Compile and save assembly code of the library.

In Figure 50, the library (highlighted area 1) is coded, which does not contain the main function of the program, since the library cannot contain the main function of the program. Once compiled, the library is created and downloaded (*Library* menu button) as shown in the highlighted areas 2.

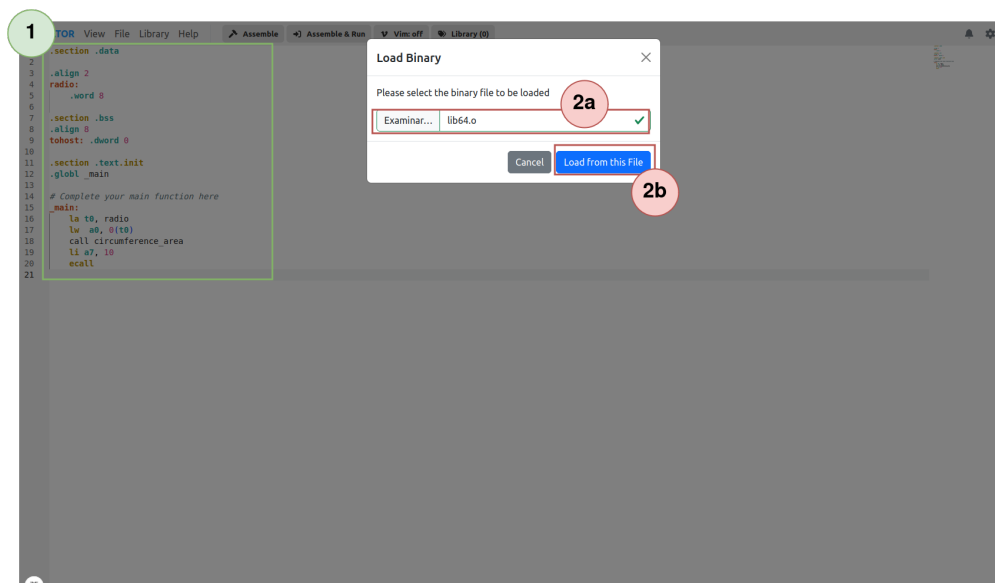


Figure 51: Import library to compile with main function.

Once the library has been generated, we proceed to import the library and encode the program, as shown in Figure 51. To do this, we select the “Load library” option from the *Library* menu and load the previously downloaded library (highlighted areas 2). Once loaded, replace the program code with that of the main function that calls the library function (highlighted area 1), compile the program, and open the simulation view to run it.

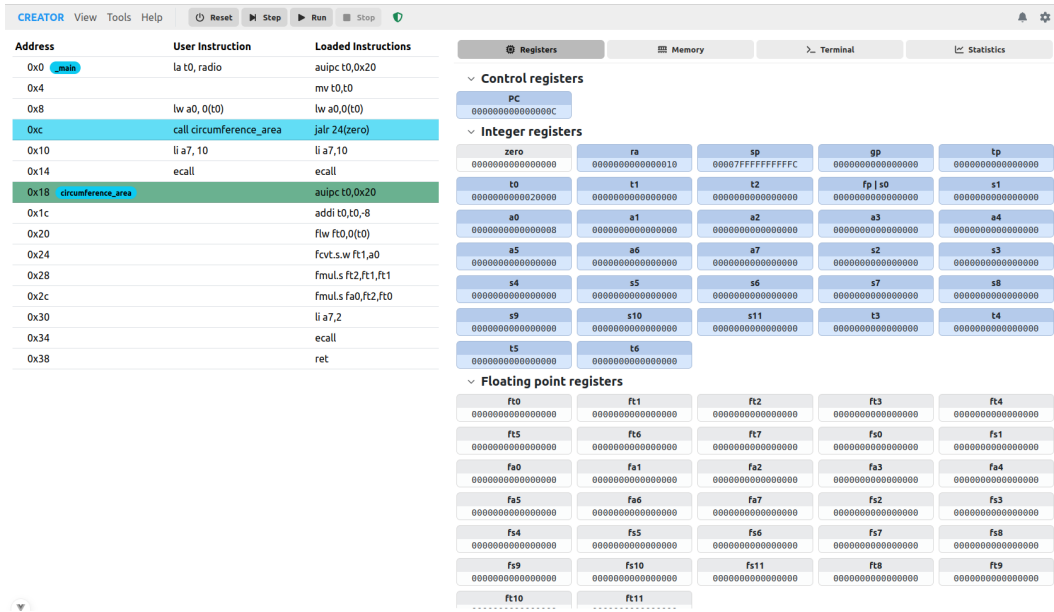


Figure 52: Execution of a binary generated with a library.

In the simulation view, the program is executed and, as shown in Figure 52, the simulator correctly executes the call from “main” to the function that calculates the area of a circle.